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Method of HyperTransport Link Probing

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Submitted a document entitled "*Method of HyperTransport Link Probing*" for consideration for inclusion into the HyperTransport Interface Design Guide

With the submission of this contribution, the submitting company agrees to all Intellectual Property terms and conditions of your agreement with the HyperTransport Technology Consortium.

Signature: Date: 5/5/05

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Method of HyperTransport Link Probing

1.0 Introduction

The HyperTransport link is 2 to 32 bits wide, with a 400 to 2800 Mbits/s transfer rate that is clocked synchronously on both rising and falling edges of the clock. Designed as a point-to-point packet-based link, HyperTransport utilizes two unidirectional signal sets between single chips on a board or between boards. Figure 1 illustrates this link.

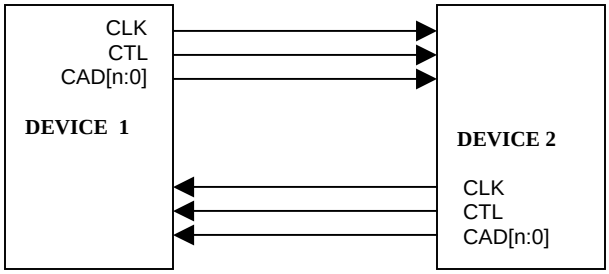


Figure 1. HyperTransport Link

Figure 2 shows the nominal voltage levels and timing of the differential HyperTransport signals. T_{CADV} is the CAD/CTL valid time relative to the CLK signal. Section 19.5 of the HyperTransport Link Specification lists the maximum and minimum values of T_{CADV} for different link speeds.

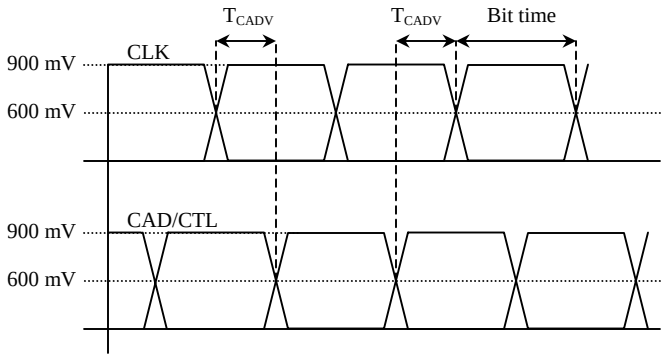


Figure 2. HyperTransport Link Signal Levels and Timing

This paper will describe a probing method designed to capture these signals and decode them for the purpose of hardware and software development.

2.0 Probing concepts

Probing methodology

Oscilloscopes and logic analyzers are the primary instruments used to probe any link. HyperTransport is no exception. Oscilloscopes are of value when looking at individual HyperTransport signals for signal integrity or pairs of signals for timing (setup and hold or skew). They are of little use when looking at groups of signals, especially on the packet level. This paper will deal with the use of a logic analyzer for HyperTransport link analysis. Digital probing with a logic analyzer involves adapting the analyzer to the HyperTransport environment in the areas of mechanical interface, electrical compatibility, timing and packet decoding.

Mechanical interface

The mechanical interface consists of one or more connectors located on the target system board that mates with a connector on the end of a ribbonized coax cable. The board connector is chosen to minimize board space. It is surface mounted to leave inner layers free for routing.

Electrical compatibility

Electrical compatibility implies that the probe should be “invisible to the link”. Loading of the link should be minimized. No signals should be introduced onto the link by the probe. The probe also has to be compatible with the logic levels of HyperTransport so that it may provide the logic analyzer with signal levels that can be captured with the minimum number of channels. The HyperTransport probe discussed herein utilizes both buffers and passive isolation techniques. This insures minimal link loading while providing logic level translation to the logic analyzer.

Timing

The HyperTransport probe needs to perform deserialization in order to capture packets and present them to the logic analyzer. To accomplish this, timing is critical and must not be distorted. Clock to data skew must be minimized. T_{CADV}, the timing of CAD/CTLOUT to CLKOUT, is defined in the HyperTransport specification Section 19.5 for a range of clock speeds. This specification must be adhered to for all the CAD/CTL lines that tap onto the HyperTransport link. Tight control of line to line skew for CAD/CTL signals is implied here. Probe design assumes that this timing will be adhered to including any additional skew introduced by circuit traces from the link taps to the connector. Probes are calibrated to minimize this skew over all the signals due to cable variations but the target board skew cannot be anticipated. That is why link tap circuit trace lengths are specified. Reference should also be made to the HyperTransport specification section M.2, PCB Skew.

Packet decoding

Packet decoding consists of deserialization of the CAD stream in the probe and the inverse assembly (decoding) of the captured CAD words to display the commands, data and CRC’s on the logic analyzer. The inverse assembler has an intimate knowledge of the HyperTransport protocol built into it.

3.0 Benefits and challenges of digitally probing HyperTransport

This section describes the benefits and the challenges faced when probing the HyperTransport link digitally.

Benefits

The first and most obvious benefit is hands free operation. The onboard connector allows the probe to be attached without holding it in place. Additionally the logic analyzer allows simultaneous viewing of activity on all lines. This is useful in top-level diagnostics for locating non-operating signals.

Another benefit of digital probing is the capture of all data lines with packet decoding via the Inverse Assembler. This facilitates hardware and code debug.

Digital probing will capture CRC's and compare them to calculated values derived from captured data. This allows faulty links to be identified.

Challenges

There are several challenges inherent in digitally probing HyperTransport. The link utilizes up to 1.4GHz differential signals with unique logic levels. This calls for special probe input buffers and differential to single-ended conversion in order to minimize the number of logic analyzer channels used. In addition, the deserialization of data requires synchronization of the master clock to the logic analyzer with the start of the data. This is handled internally to the probe hardware with a synchronization circuit that keys off the start of data.

Another challenge involves maintaining the signal integrity of the link both with and without the probe attached to the target board connector. Furthermore the data to clock skew in both the probe and the link attachment must be minimized.

The CRC codes in HyperTransport present a unique challenge. The CRC codes appear every 512 bit times and can occur in the middle of packets. The inverse assembler must be able to identify these codes as well as calculate them for the preceding data. These codes occur with the CTL bit asserted and can therefore masquerade as commands. The inverse assembler must allow the selection of a bit time when the CRC occurs. The inverse assembler can then identify all the commands that occur on 512 bit time boundaries as CRC's, with the selected CRC bit time used as the index point. Simply stated, if you find a CRC then 512 bit times later another will occur.

4.0 Signal integrity issues and solutions

The signal integrity issues involve HyperTransport link loading and CAD/CTL to CLK signal skew from the link into the probe input registers. This paper shall address the signal chain in light of these issues and present solutions.

The circuit from the link to the probe connector shall be discussed first. Link loading must be minimized to the point where the probe is electrically invisible to the link. There must also be minimal impact with the probe cable disconnected. This means that the impedances of the tap points should be high and no stub effects should be apparent at the frequencies involved.

The implementation that provides the best solution to the above issues has the following criteria:

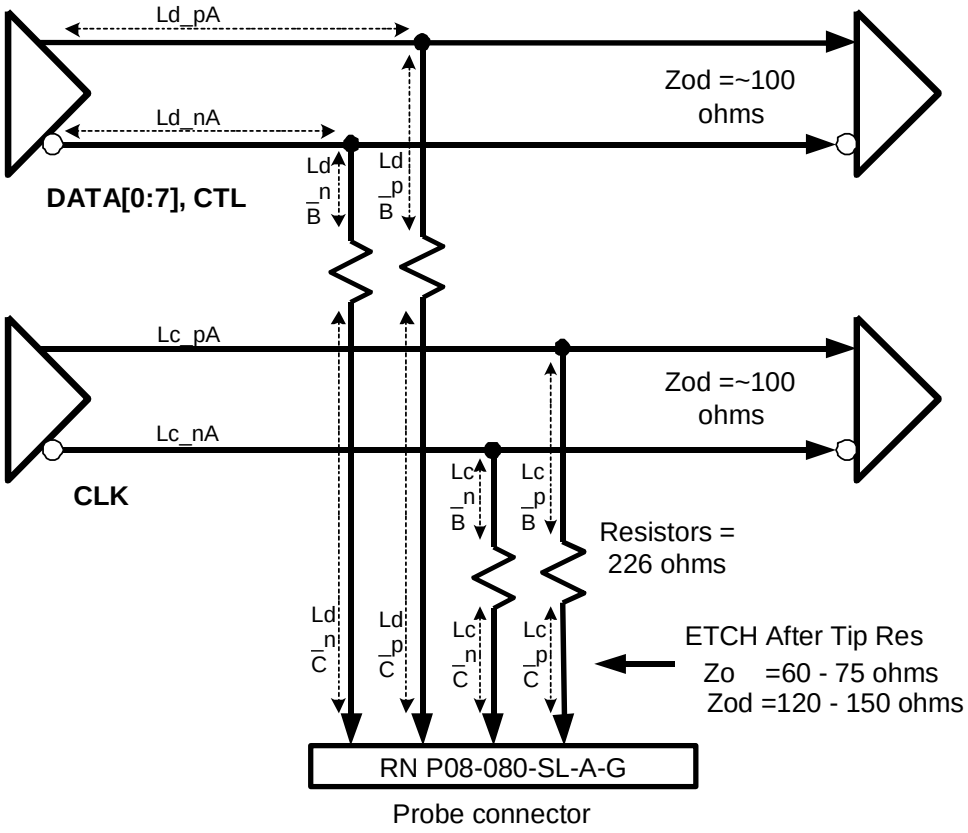
1. Delays of signals from the driving device to the connector are equalized
2. The maximum etch length from target signal to the connector is controlled
3. The stub length of the etch from target signal to the tip resistors is minimized
4. Tip resistors are chosen by simulation to provide a best match between the probe and the HyperTransport link on the target board

Figure 3 on the next page shows the parameters, with the constraints tabled below it, that provide an optimal solution. In some situations, the lengths from the tip resistors to the connector can be longer, but a simulation run is advised to assess the impact. Tip isolation resistors of 226 ohms were found to be the best value through SPICE simulations. (The simulations included the cable, probe board and input buffers are discussed in the next section.) It should be noted at this point that discussion has assumed continuous traces from link tap to connector. As a practical matter, this is never the case. Resistors and associated pads exhibit a lumped capacitance to ground that is higher than the distributed capacitance of an equal length of circuit trace. The use of vias contributes a series inductance as well as capacitance to ground. These factors should be included in simulations of particular layouts. More information on the simulations will be presented later on in this section.

The next piece of the signal integrity issue involves the path from the connector to probe input buffers via the ribbonized coax cable. As previously mentioned, connectors must minimize impedance discontinuities and be capable of passing the maximum frequencies expected for HyperTransport. This controls reflections and stub effects. The cable frequency response must support HyperTransport. The skew in the coax cables is due to mechanical path differences and is difficult to precisely control.

Input signal levels to the probe are attenuated and buffering is required. The buffers exhibit different propagation delay times and hence cause skew. Skew on the probe circuit board is caused by mechanical path differences, uneven capacitive loading of individual signals (slowing the rise time and creating skew) and semiconductor device delay variations. Calibration of the HyperTransport probe adjusts the CLK to CAD/CTL skew so that the setup and hold times for the input registers are met.

HT Probe Etch Length Rules



Data to Clock Length Matching

[Ld_pA + Ld_pB + Ld_pC] - [Lc_pA + Lc_pB + Lc_pC] = 0 +/- 0.020”

Diff Pair Length Matching

[Ld_pA + Ld_pB + Ld_pC] - [Ld_nA + Ld_nB + Ld_nC] = 0 +/- 0.020”

[Lc_pA + Lc_pB + Lc_pC] - [Lc_nA + Lc_nB + Lc_nC] = 0 +/- 0.020”

Maximum Etch Length Rules

Driver to Probe Connector : [Ld_pA + Ld_pB + Ld_pC] < 4.0”

and [Lc_pA + Lc_pB + Lc_pC] < 4.0”

Etch to Tip R Stub [Ld_pB or Ld_nB or Lc_pB or Lc_nB] < 0.050”

Figure 3 Etch Length Rules for HyperTransport Probe Connector Attachment

Note: For HT Link speeds at ≤ 800MT/s, these tolerances double and the maximum etch to tip R stub can be ≤ 0.100”

5.0 Simulations of HyperTransport Probing

The information presented below constitutes the SPICE models and simulation used to predict HyperTransport link probing. Figure 4 shows the simulation results at a HyperTransport receiver with tip resistors depopulated. Figure 5 shows the results with tip resistors installed but probe cable detached. Figure 6 displays the result with the probe attached and operating.

Simulation models

This section lists the SPICE models for the various subcircuits that were used to model the HyperTransport probing and derive the results shown at the end of this section.

HyperTransport driver:

HyperTransport receiver:

HyperTransport link etch:

Link tap etch:

Tip resistors:

Tip resistor to connector etch:

Connector:

Coax ribbon cable:

Probe board:

Probe buffers:

SPICE Simulation

The SPICE simulation will ultimately contain vendor models that are likely to be proprietary as well as circuit board models that are layout specific. For these reasons the simulation listing for the results in Figs. 4, 5, and 6 is not presented here.

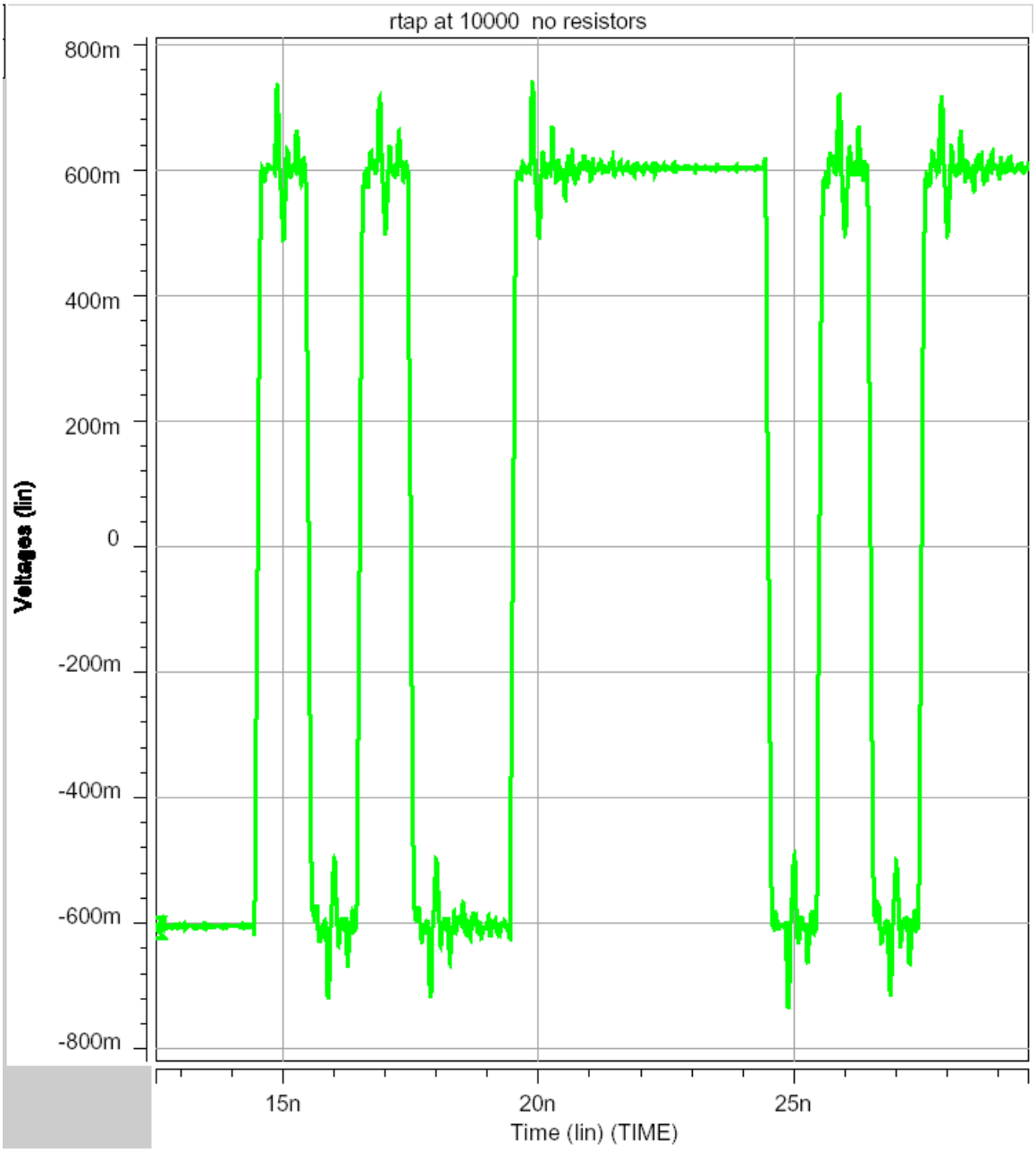


Figure 4 HT link Without Tip Resistors (Differential Signal at HT Receiver)

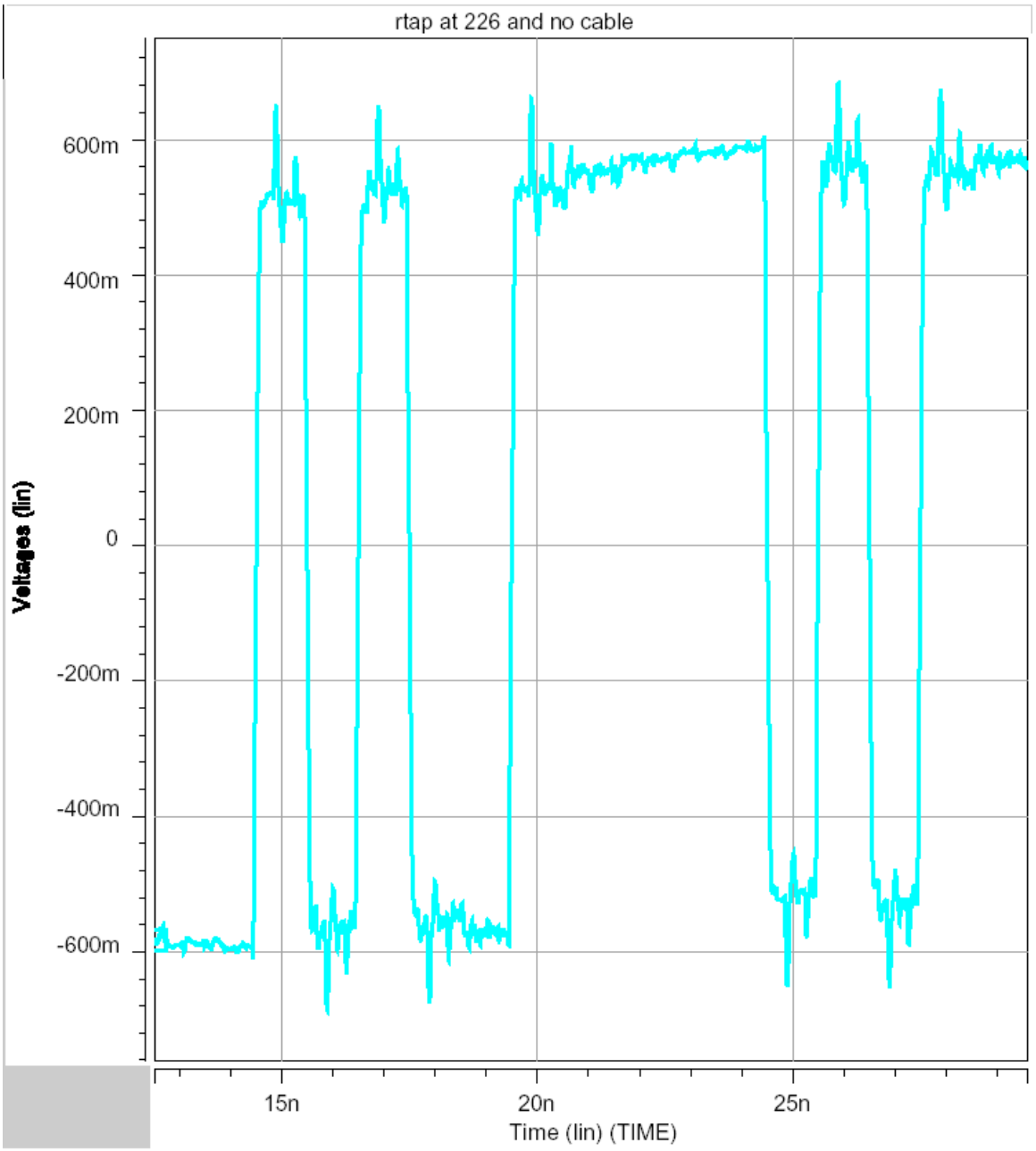


Figure 5 Resistors In and Cable Detached (Differential Signal at HT Receiver)

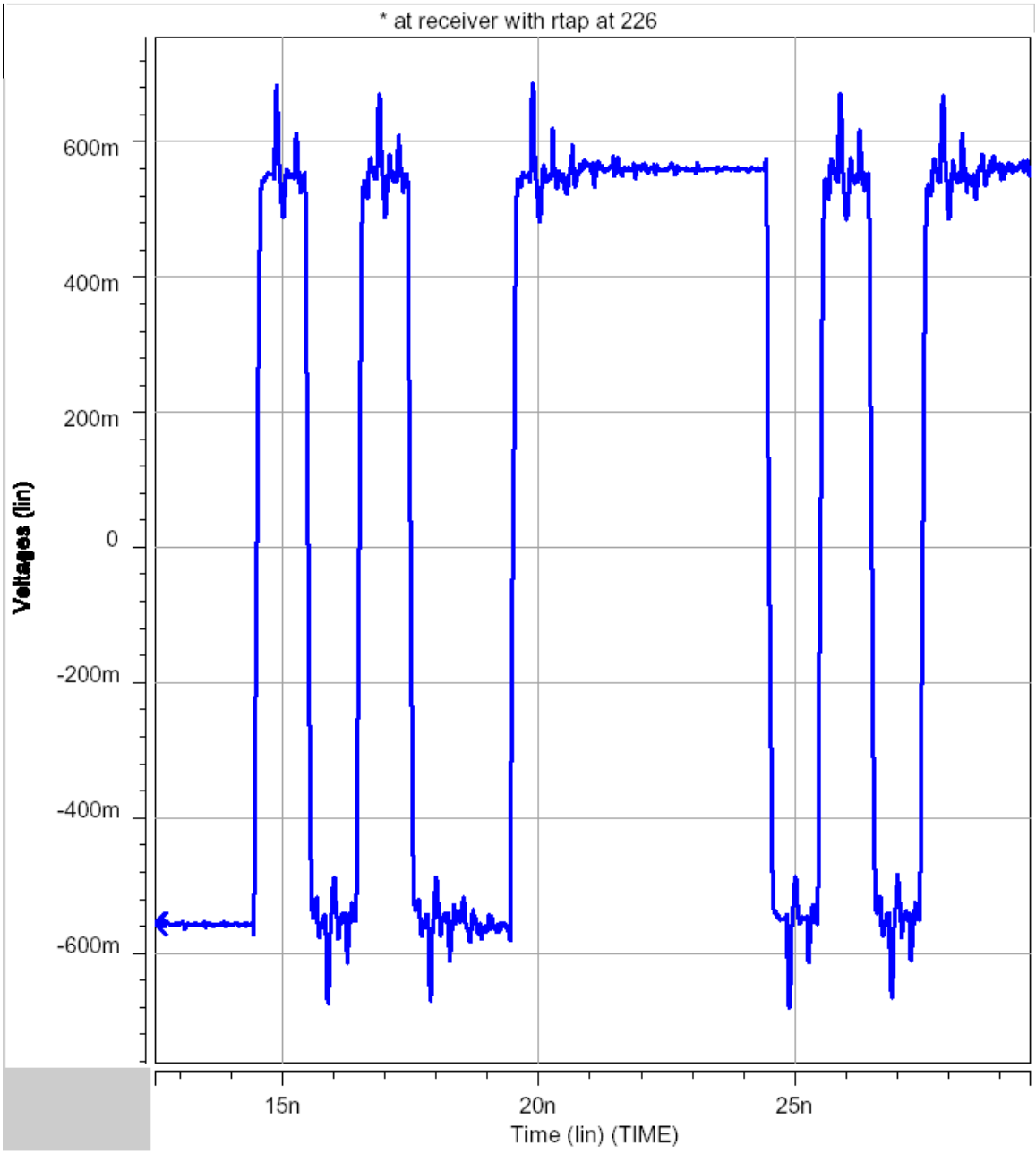


Figure 6 HT Probe attached (Differential Signal at HT Receiver)

6.0 Putting it all together

Method of probing

The method of probing discussed in this paper is digital in nature and uses isolation resistors and a buffered active probe with deserialization. Packet decoding is accomplished in the logic analyzer employing a protocol decoder that keys off of CRC's.

Test connector pinout and placement

Figure 7 below shows the pin numbering and pad information for a Robinson Nugent p/n P08-080-SL-A-G socket that is recommended for connecting to the probe cable connector. It is a surface mounted connector that is small in size and uses a minimal number of pads for a 16 bit probe. The threaded inserts are used to retain the cable to the board. Their use is optional, but strongly recommended.

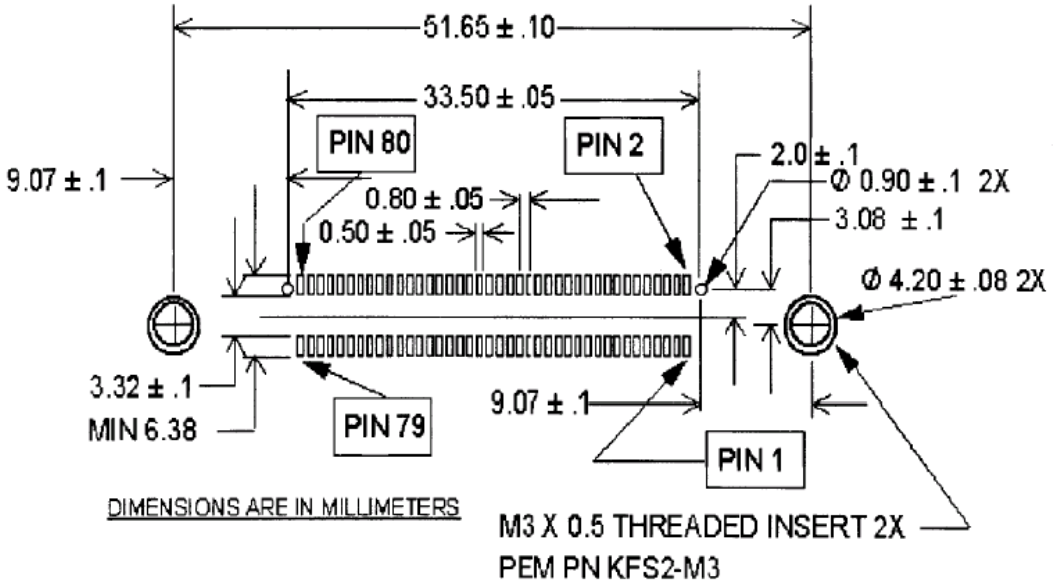


Figure 7 Pad information for probe connector

Figure 8 shows the dimensions of the cable connector end. This defines a keep out area on the target board for components.

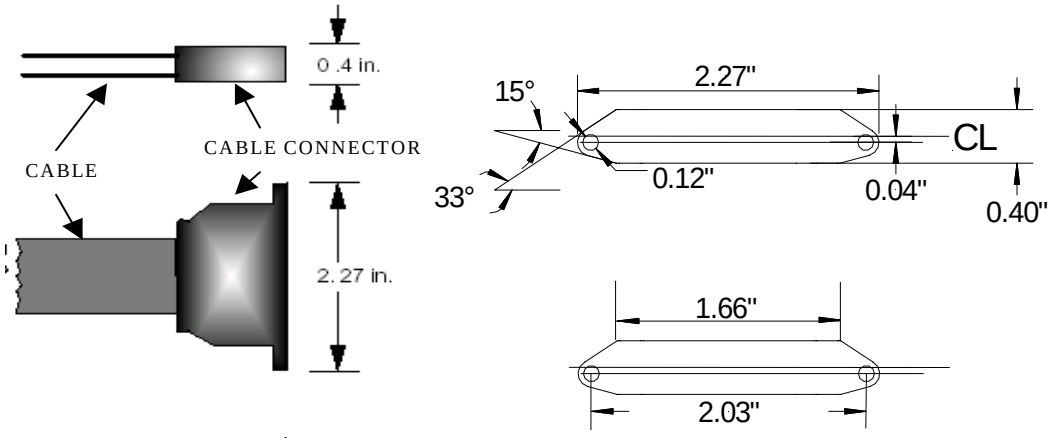


Figure 8 Cable Connector Dimensions that Determine Keep Out Area

Routing information

8 Bit Connector Layout

Table 1 below shows the 8 bit HyperTransport Robinson Nugent Connector Pin Signal List. Note that the CTL and CLK signals cannot be moved. The CAD signal pairs can be swapped with other CAD signal pairs; however, do not change the relative _H/_L pin assignment.

16 Bit Connector Layout

Table 2 below lists the 16 bit HyperTransport Robinson Nugent Connector Pin Signal List. Note that the CTL and CLK signals cannot be moved. The CAD[0-7] signal pairs can be swapped with other CAD[0-7] signal pairs and CAD[8-15] signal pairs can be swapped with other CAD[8-15] signal pairs, however, do not change the relative _H/_L pin assignment. The BIAS pin should be connected to a 1K ohm resistor to ground (pull down). Upper clock is the clock for bits 15-8. Lower clock is the clock for bits 7-0.

Signal Name	Pin #	Pin #	Signal Name
RESET# (optional)	1	2	PWROK (optional)
LDTSTOP# (optional)	3	4	LDTREQ# (optional)
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
RX_CAD_L[0]	11	12	TX_CAD_L[0]
RX_CAD_H[0]	13	14	TX_CAD_H[0]
GND	15	16	GND
RX_CAD_L[1]	17	18	TX_CAD_L[1]
RX_CAD_H[1]	19	20	TX_CAD_H[1]
GND	21	22	GND
RX_CAD_H[2]	23	24	TX_CAD_H[2]
RX_CAD_L[2]	25	26	TX_CAD_L[2]
GND	27	28	GND
RX_CAD_H[3]	29	30	TX_CAD_H[3]
RX_CAD_L[3]	31	32	TX_CAD_L[3]
GND	33	34	GND
RX_CTL_L	35	36	TX_CTL_L
RX_CTL_H	37	38	TX_CTL_H
GND	39	40	GND
RX_CLK_H	41	42	TX_CLK_H
RX_CLK_L	43	44	TX_CLK_L
GND	45	46	GND
RX_CAD_H[4]	47	48	TX_CAD_H[4]
RX_CAD_L[4]	49	50	TX_CAD_L[4]
GND	51	52	GND
RX_CAD_H[5]	53	54	TX_CAD_H[5]
RX_CAD_L[5]	55	56	TX_CAD_L[5]
GND	57	58	GND
RX_CAD_L[6]	59	60	TX_CAD_L[6]
RX_CAD_H[6]	61	62	TX_CAD_H[6]
GND	63	64	GND
RX_CAD_L[7]	65	66	TX_CAD_L[7]
RX_CAD_H[7]	67	68	TX_CAD_H[7]
GND	69	70	GND
GND	71	72	GND
GND	73	74	GND
GND	75	76	GND
GND	77	78	GND
GND	79	80	GND

Do not ground pins 1 - 4

Table 1 8 bit HyperTransport Robinson Nugent Connector Pin Signal List

Signal Name	Pin #	Pin #	Signal Name
RESET# (optional)	1	2	PWROK (optional)
LDTSTOP# (optional)	3	4	LDTREQ# (optional)
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
CAD_L[8]	11	12	CAD_L[0]
CAD_H[8]	13	14	CAD_H[0]
GND	15	16	GND
CAD_L[9]	17	18	CAD_L[1]
CAD_H[9]	19	20	CAD_H[1]
GND	21	22	GND
CAD_H[10]	23	24	CAD_H[2]
CAD_L[10]	25	26	CAD_L[2]
GND	27	28	GND
CAD_H[11]	29	30	CAD_H[3]
CAD_L[11]	31	32	CAD_L[3]
GND	33	34	GND
GND	35	36	CTL_L
BIAS	37	38	CTL_H
GND	39	40	GND
UPPER_CLK_H	41	42	LOWER_CLK_H
UPPER_CLK_L	43	44	LOWER_CLK_L
GND	45	46	GND
CAD_H[12]	47	48	CAD_H[4]
CAD_L[12]	49	50	CAD_L[4]
GND	51	52	GND
CAD_H[13]	53	54	CAD_H[5]
CAD_L[13]	55	56	CAD_L[5]
GND	57	58	GND
CAD_L[14]	59	60	CAD_L[6]
CAD_H[14]	61	62	CAD_H[6]
GND	63	64	GND
CAD_L[15]	65	66	CAD_L[7]
CAD_H[15]	67	68	CAD_H[7]
GND	69	70	GND
GND	71	72	GND
GND	73	74	GND
GND	75	76	GND
GND	77	78	GND
GND	79	80	GND

Do not ground pins 1 - 4

Table 2 16 bit HyperTransport Robinson Nugent Connector Pin Signal List

Alternate Probing Connectors

Alternate connectors for probing a HyperTransport link are available, which may be more useful for probing 4 layer target boards. This is because the alternate probe designs use 2 smaller connectors and place the tip resistors on the probe cable instead of on the target. The drawback of this approach is that the application of the Etch Length Rules detailed earlier in this document is harder to achieve because of the added length through the connector to the tip resistors on the cable, and the unequal trace lengths established by placing the connector pins directly on top of the HyperTransport link etches. Because of the smaller connector size of this alternate approach, each connector provides only 8 data bits, 1 CTL, and 1 CLK signal.

This design uses 2

Pin	Signal		Signal	Pin
		Gnd		
1	CAD_H(0)		LDTREQ_L	2*
3	CAD_L(0)		LDTSTOP_L	4*
5	nc		CAD_H(4)	6
7	nc		CAD_L(4)	8
9	CAD_H(1)		nc	10
11	CAD_L(1)		nc	12
13	nc		CAD_H(5)	14
15	nc		CAD_L(5)	16
17	CAD_H(2)		nc	18
19	CAD_L(2)		nc	20
21	nc		CAD_H(6)	22
23	nc		CAD_L(6)	24
25	CAD_H(3)		nc	26
27	CAD_L(3)		nc	28
29	nc		CAD_H(7)	30
31	nc		CAD_L(7)	32
33	CLK_H		nc	34
35	CLK_L		nc	36
37	Gnd		CTL_H	38
39	nc		CTL_L	40
		Gnd		

* PWR_OK and LDTRST_L are probed on pin 2 and 4 respectively of the Input 1 connector.
Either Input 0 or 1 can be used for Transmit or Receive data. However, these signals on pins 2 and 4 are fixed.

Table 3 8 bit HyperTransport Samtec probe F configuration Input 0 Pin Signal List

The H configuration of the probe connector is more suitable for HyperTransport links where all 8 bits are routed on the same layer of the pcb. In this situation the connectors should be on the side of the pcb with the signals.

Pin	Signal		Signal	Pin
		Gnd		
1*	PWR_OK		CTL_L	2
3*	LDTRST_L		CTL_H	4
5	CAD_L(7)		nc	6
7	CAD_H(7)		nc	8
9	nc		CAD_L(6)	10
11	nc		CAD_H(6)	12
13	CAD_L(5)		nc	14
15	CAD_H(5)		nc	16
17	nc		CAD_L(4)	18
19	nc		CAD_H(4)	20
21	CLK_L		nc	22
23	CLK_H		nc	24
25	nc		CAD_L(3)	26
27	nc		CAD_H(3)	28
29	CAD_L(2)		nc	30
31	CAD_H(2)		nc	32
33	nc		CAD_L(1)	34
35	nc		CAD_H(1)	36
37	CAD_L(0)		Gnd	38
39	CAD_H(0)			40
		Gnd		

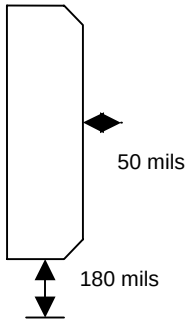
* LDTREQ_L and LDTSTOP_L are probed on pin 1 and 3 respectively of the Input 1 connector.
Either Input 0 or 1 can be used for Transmit or Receive data. However, these signals on pins 1 and 3 are fixed

Table 4 8 bit HyperTransport Samtec H configuration Input 0 Pin Signal List

The Samtec QSH-020-DP connector has a center ground conductor, which should only be connected at the ends (pins 1, 2, 39, and 40) of the connector. The pads for this ground conductor should be made as large as possible without interfering with the path of the signals on the HyperTransport link.

Note: There is a possibility that the center conductor of the connector, or unused and unsoldered connector pins may over time wear through the soldermask of the target board and create an intermittent connection to signals. In order to prevent this, carefully inspect the solder mask on the target board before soldering the connector. A thin strip of Kapton tape over the unsoldered areas of the center conductor may provide additional mechanical protection.

Keepout Requirements – There should be no components within 180 mils of ends of the connector and within 50 mils of the long sides.



Samtec Connector layout – The recommended connector to use is a Samtec QSH-020-01-L-D-DP-K. The .020” pitch of the connector allows pads to be placed on the standard HT link layout without changing the 5 mil spacing of a differential pair. This minimizes the impact to a target board design when implementing a probe connection.

Connector and footprint information can be found at www.samtec.com. The pad layout for the QSH-020-DP is shown below. It is recommended to leave out the pads for no connects as they can interfere with routing the HT signals. The connector should be oriented so that the side with the chamfered corners be pointing away from the receiver. Vias to bring signals from the opposite side of the board should be made as small as possible.

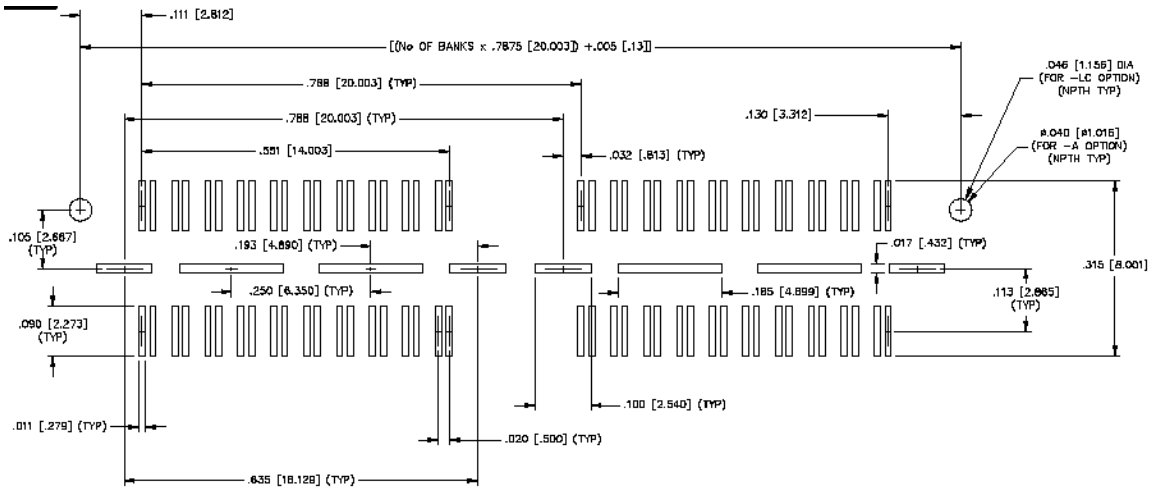


Figure 9 Samtec QSH – DP connector footprint.

Two aspects of this alternate probe design impact it's use above 400MT/s. The first is the fact that because the tip resistors are placed across the QSH/QTH mated pair they are 0.485" away from the QSH connector pads on the HyperTransport target. The second impact is that because the connector is placed directly on the HyperTransport Link there can be a small difference in the lengths of the differential pairs on one side of the connector when compared to the other. Figure 10 shows a Probe F configuration on a target board. Note that the differential pairs for CAD1 (left column of pads) are probing the Link at a different location than where CAD4 (right column of pads) is probed. This difference is based on 2 factors:

1. The spacing from the center of the left pads to the center of the right pads, which is 0.226".
2. The difference in connection points to the HT trace for each signal. For example, in the layout below. CAD0 has the shortest Length A (reference figure 3)

Adjusting etch lengths to the connector pads to minimize these length differences along with simulation of the connection at target speeds above 400MT/s is recommended.

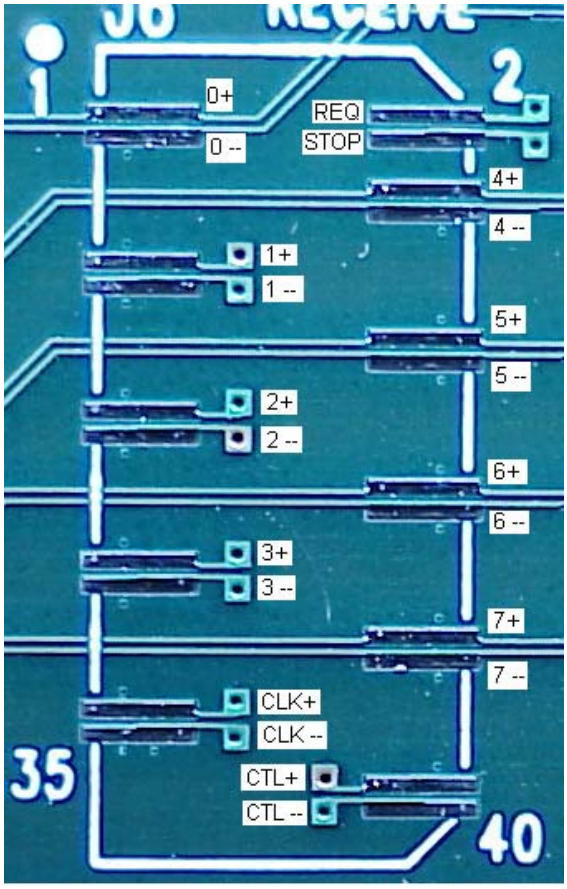


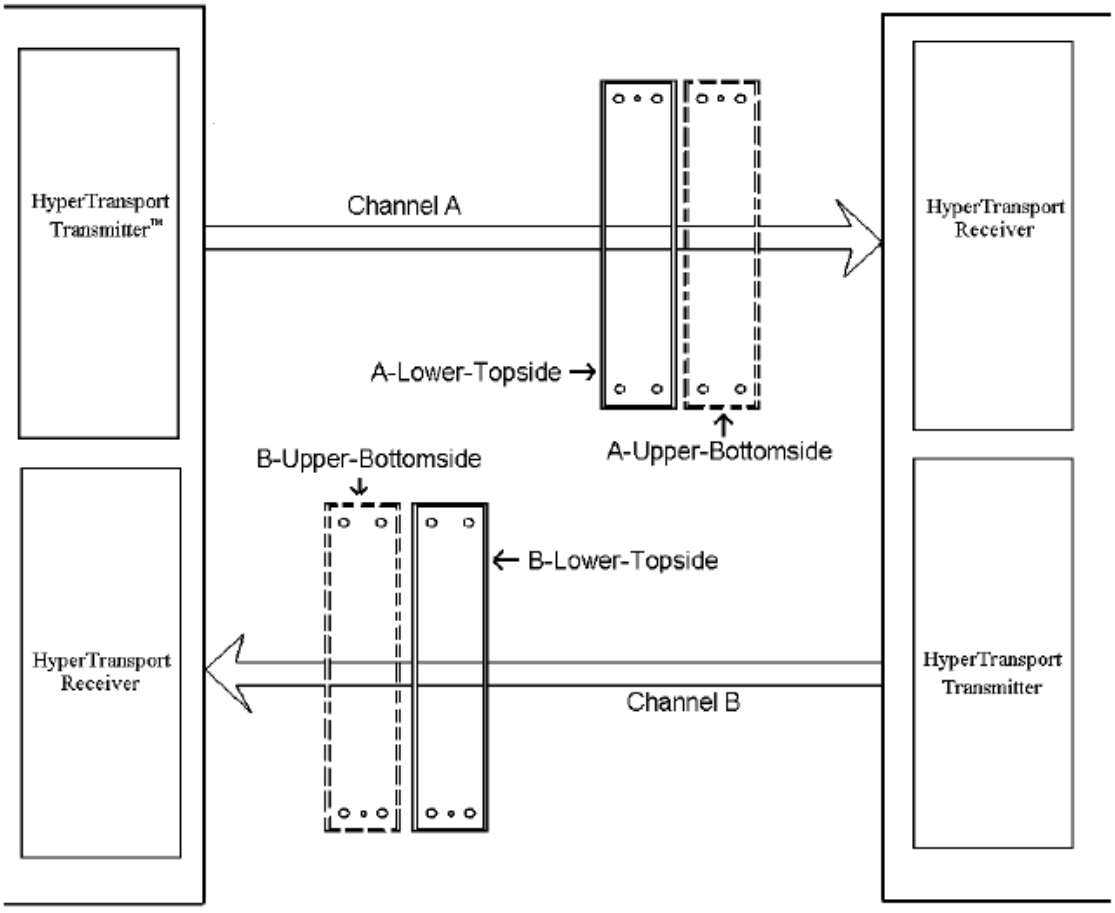
Figure 10 – Samtec connector layout on target
(Note: There are no pads for center ground connection on this layout)

Connectorless Method of Probing – FS2243

Another probing approach uses a “connectorless” approach for probing HyperTransport links. This method is easier to implement on targets with low layer counts and/or tight space requirements, because it does not require tip resistors on the target and only brings 10 bits to each of the 2 probing locations required per link. Additionally, it can be implemented using standard PCB pad features and can therefore be designed into a target board at no cost increase and used when needed with little additional commitment of time and money.

In order to probe 8 bit (TX **and** RX) or a 16 bit HT link (TX **or** RX), 2 separate connectorless probing locations are needed. The overall placement strategy is to place one of each of the probing locations on each side of the board as close as possible to the Receive end of the link. It is recommended that A Lower and B Lower be placed on the top side and A and B Upper be placed on the bottom side of the target board.

This layout was designed to minimize the impact of probing a HT link utilizing a microstrip layout where the upper and lower bytes are routed on different layers.



NOTE – dashed lines for “Upper-Bottomside” connectors for use when probing TX and RX on 16 bit links

probing footprint

The footprint designed for use with this probing approach is shown below in *Figure 11*: Please note that not all probe pads are required, reference the A and B, Upper and Lower pinouts described in this document.

Layout guidelines:
Vias in pads are not recommended. A via that is tangential to the pad is allowed. There must be a solder mask between all pads. Recommended pad finish is HASL, immersion silver, or gold over nickel.

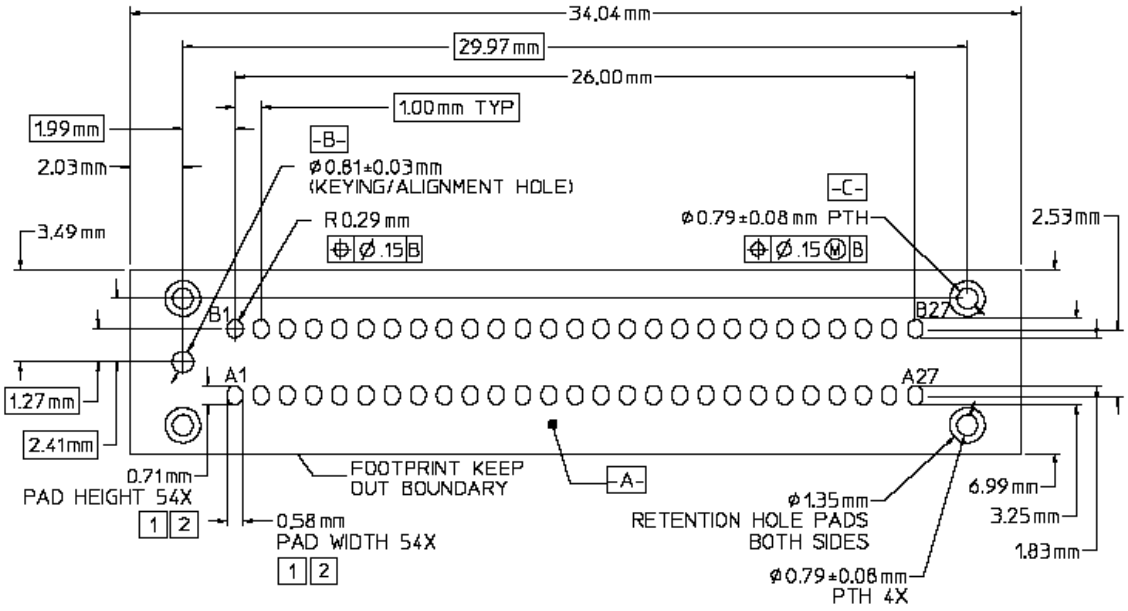


Figure 11 – Mechanical layout for connectorless probing

Retention module

A retention module (*Figure 12*) is required to provide the mechanical support of the connectorless probe to the target board. The module is simply attached to the board by soldering its legs to the plated through holes that are part of the footprint described above. The probe is then connected to the target by placing the probe head into the retention clip, taking care to maintain polarity, and screwing down the captive fasteners.

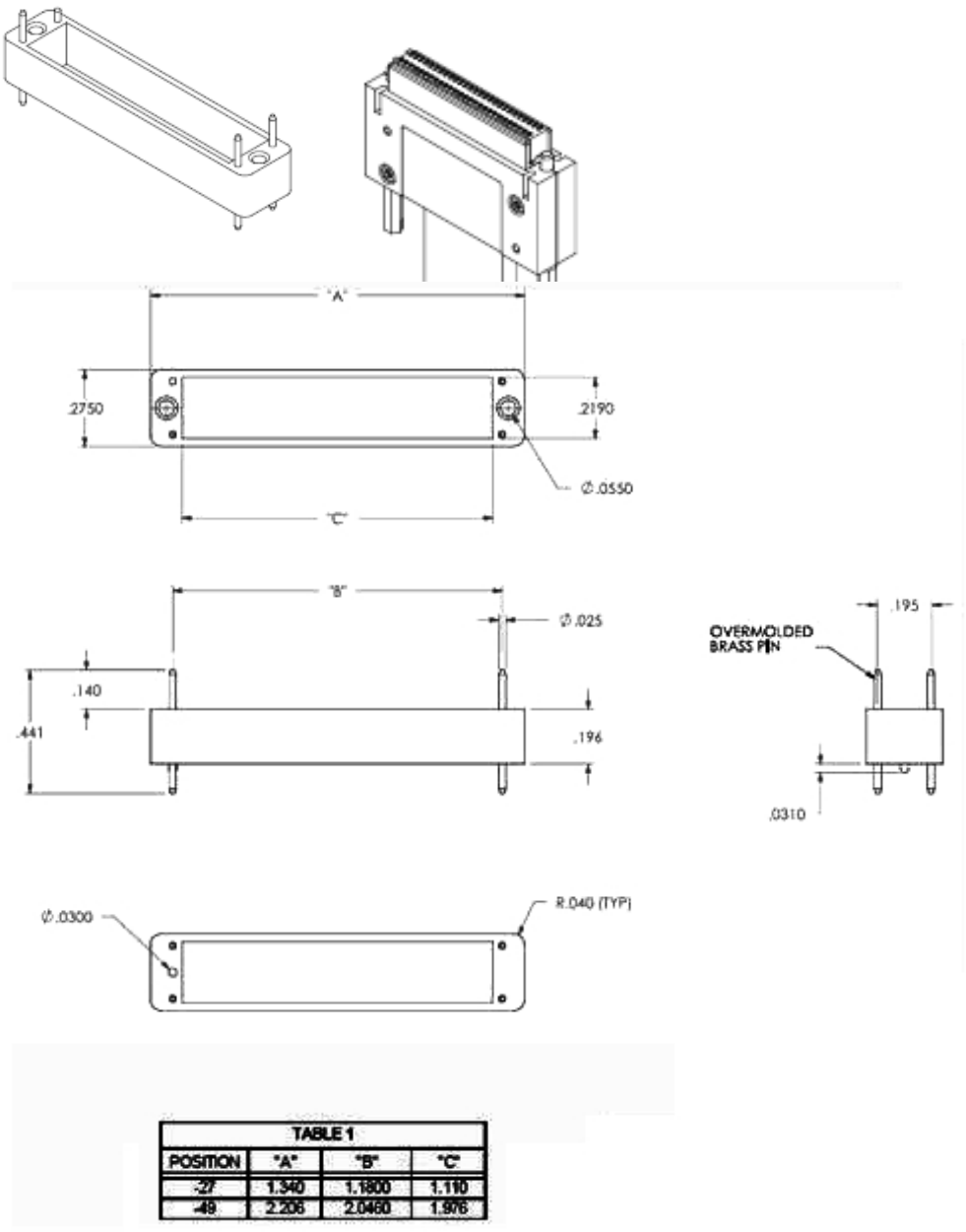
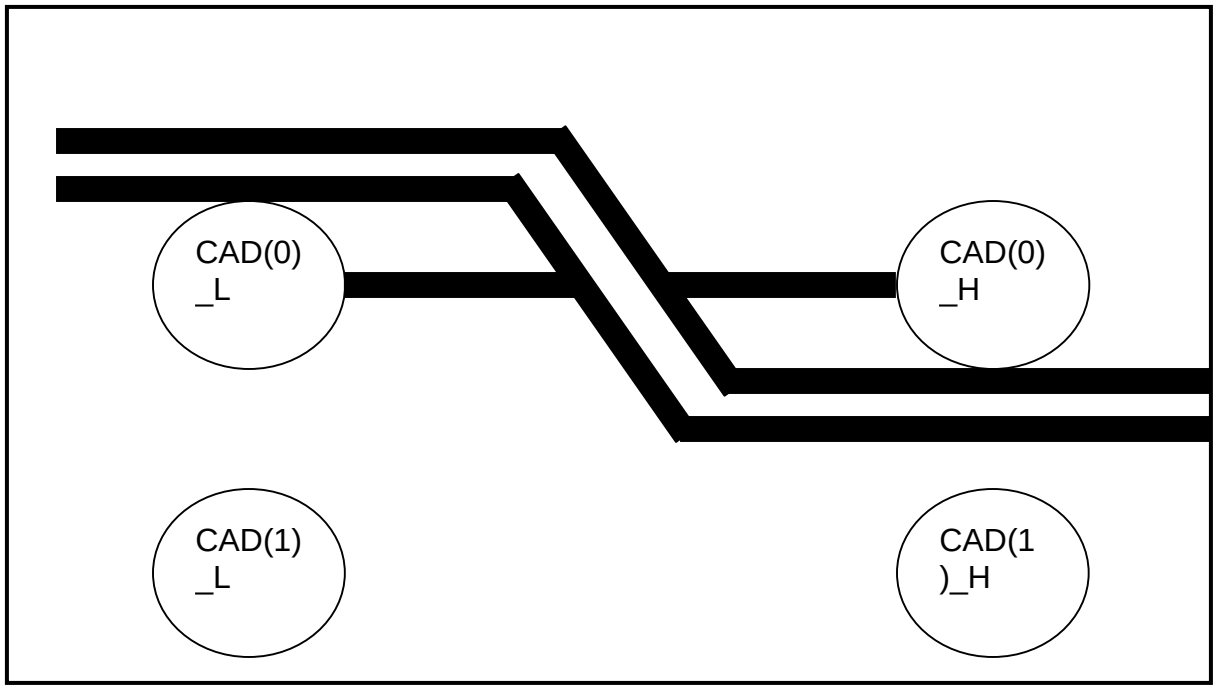


TABLE 1			
POSITION	"A"	"B"	"C"
-27	1.340	1.1800	1.110
-49	2.206	2.0460	1.976

Figure 12 – Retention Module

Connectorless probe trace routing – Differential signals in same row different columns

The goal is to minimize the disruption to the standard HT differential pair routing between devices and to minimize any differences in position on the link where each signal is probed, as well as introduce only a minimal and equal length stub to each pad. It is also important to maintain the 5 mil spacing between signals in a pair. The following is an example of a layout for 1 pair where the signals are in the same row but different columns.

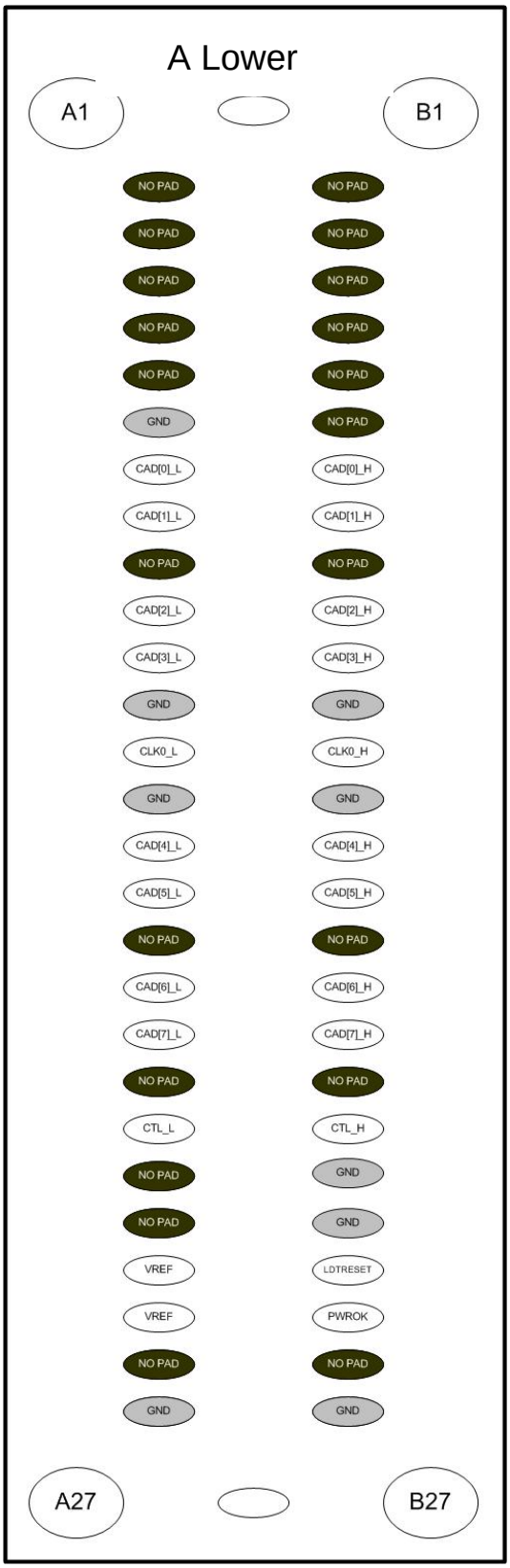


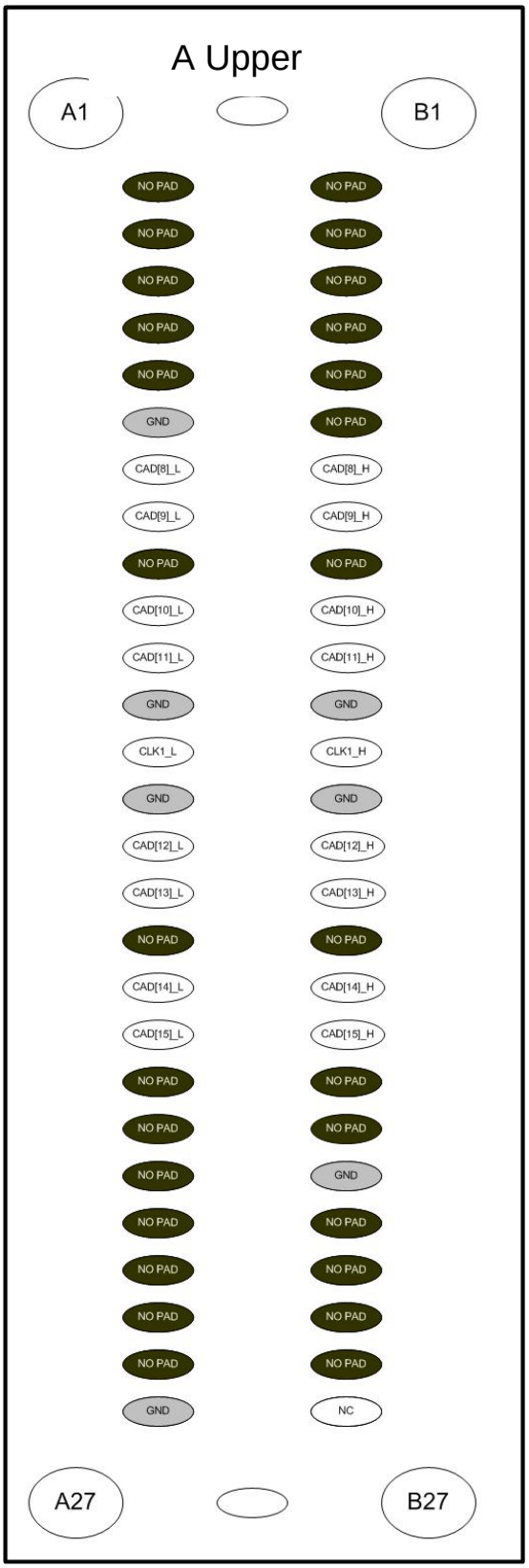
The following pages show a detailed pin out for 4 probing connections required for capturing both Receive and Transmit traffic simultaneously on a 16 bit HT link.

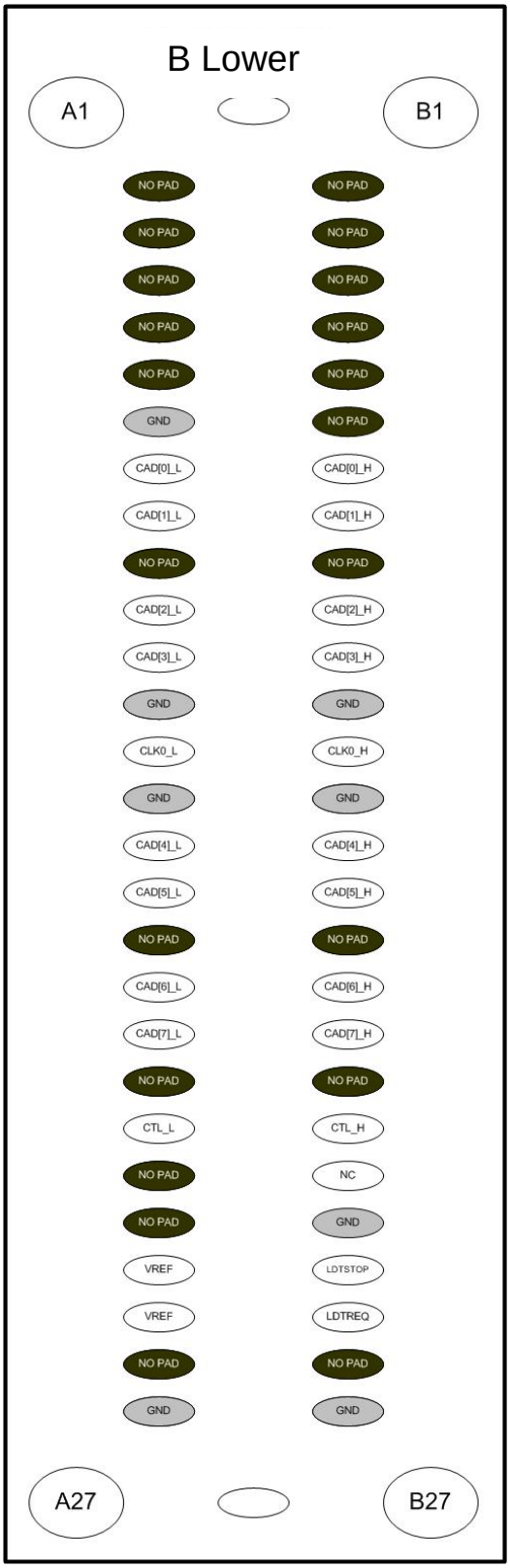
For 8 bit TX and RX data capture use A Lower for TX and B Lower for RX.

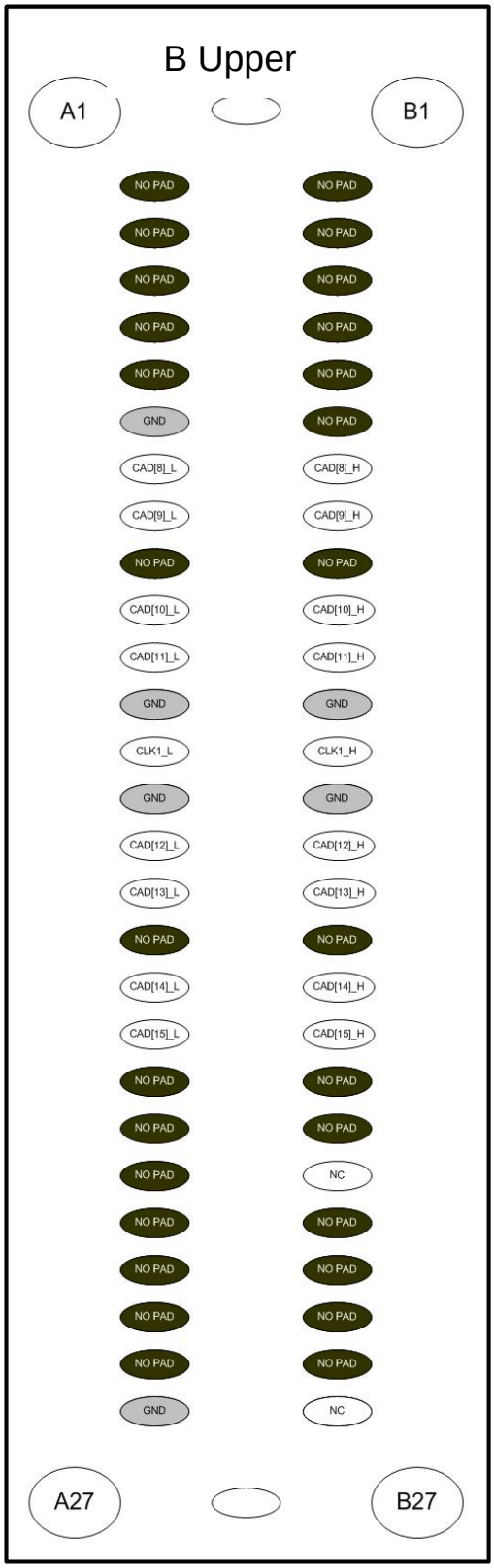
For 16 bit TX only, two probing connections are required – A Lower and A Upper.
For 16 bit RX only, two probing connections are required – B Lower and B Upper.

The following diagrams describe certain probing positions as “NO PAD” and others and “NC”. NC indicates the presence of a pad but no connection to circuitry. NO PAD indicates that there is no physical pad on the board. Only pads with signal names need to be created on the board, which may ease trace routing.


A Lower
A1
B1
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
GND
CAD[0]_L
CAD[1]_L
NO PAD
CAD[2]_L
CAD[3]_L
GND
CLK0_L
GND
CAD[4]_L
CAD[5]_L
NO PAD
CAD[6]_L
CAD[7]_L
NO PAD
CTL_L
NO PAD
NO PAD
VREF
VREF
NO PAD
GND
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
CAD[0]_H
CAD[1]_H
NO PAD
CAD[2]_H
CAD[3]_H
GND
CLK0_H
GND
CAD[4]_H
CAD[5]_H
NO PAD
CAD[6]_H
CAD[7]_H
NO PAD
CTL_H
GND
GND
LDTRESET
PWROK
NO PAD
GND
A27
B27


A Upper
A1
B1
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
GND
CAD[8]_L
CAD[9]_L
NO PAD
CAD[10]_L
CAD[11]_L
GND
CLK1_L
GND
CAD[12]_L
CAD[13]_L
NO PAD
CAD[14]_L
CAD[15]_L
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
GND
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
CAD[8]_H
CAD[9]_H
NO PAD
CAD[10]_H
CAD[11]_H
GND
CLK1_H
GND
CAD[12]_H
CAD[13]_H
NO PAD
CAD[14]_H
CAD[15]_H
NO PAD
NO PAD
GND
NO PAD
NO PAD
NO PAD
NO PAD
NC
A27
B27


B Lower
A1
B1
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
GND
CAD[0]_L
CAD[1]_L
NO PAD
CAD[2]_L
CAD[3]_L
GND
CLK0_L
GND
CAD[4]_L
CAD[5]_L
NO PAD
CAD[6]_L
CAD[7]_L
NO PAD
CTL_L
NO PAD
NO PAD
VREF
VREF
NO PAD
GND
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
CAD[0]_H
CAD[1]_H
NO PAD
CAD[2]_H
CAD[3]_H
GND
CLK0_H
GND
CAD[4]_H
CAD[5]_H
NO PAD
CAD[6]_H
CAD[7]_H
NO PAD
CTL_H
NC
GND
LDTSTOP
LDTREQ
NO PAD
GND
A27
B27

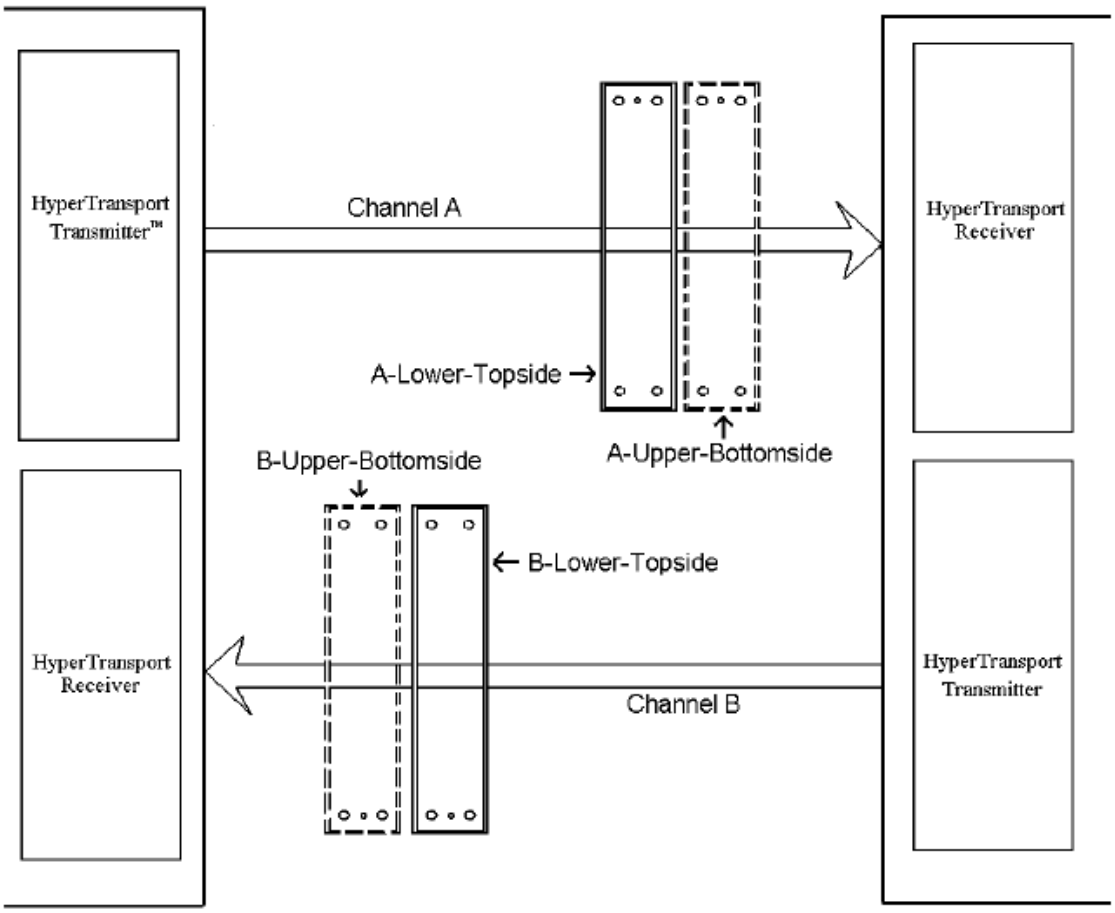

B Upper
A1
B1
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
GND
CAD[8]_L
CAD[9]_L
NO PAD
CAD[10]_L
CAD[11]_L
GND
CLK1_L
GND
CAD[12]_L
CAD[13]_L
NO PAD
CAD[14]_L
CAD[15]_L
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
GND
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
NO PAD
CAD[8]_H
CAD[9]_H
NO PAD
CAD[10]_H
CAD[11]_H
GND
CLK1_H
GND
CAD[12]_H
CAD[13]_H
NO PAD
CAD[14]_H
CAD[15]_H
NO PAD
NO PAD
NC
NO PAD
NO PAD
NO PAD
NO PAD
NC
A27
B27

Industry-Standard Connectorless Method of Probing

Another probing approach uses an “Industry-Standard connectorless” approach for probing HyperTransport links. This is similar to the technology and approach described for the previous probe, but it differs in its geometry and its pinout. Like the previous approach, this method is easier to implement on targets with low layer counts and/or tight space requirements, because it does not require tip resistors on the target and only brings 10 bits to each of the 2 probing locations required per link. Additionally, it can be implemented using standard PCB pad features and can therefore be designed into a target board at no cost increase and used when needed with little additional commitment of time and money.

Refer to the discussion in the previous section for placement of the probing locations.

This layout was designed to minimize the impact of probing a HT link utilizing a microstrip layout where the upper and lower bytes are routed on different layers.



Industry-Standard Connectorless probing footprint

The footprint designed for use is shown below in *Figure 11*: Please note that not all probe pads are required, reference the Lower and Upper pinouts described in this document.

Layout guidelines:
Vias in pads are not recommended. A via that is tangential to the pad is allowed. There must be a solder mask between all pads. Recommended pad finish is HASL, immersion silver, or gold over nickel.

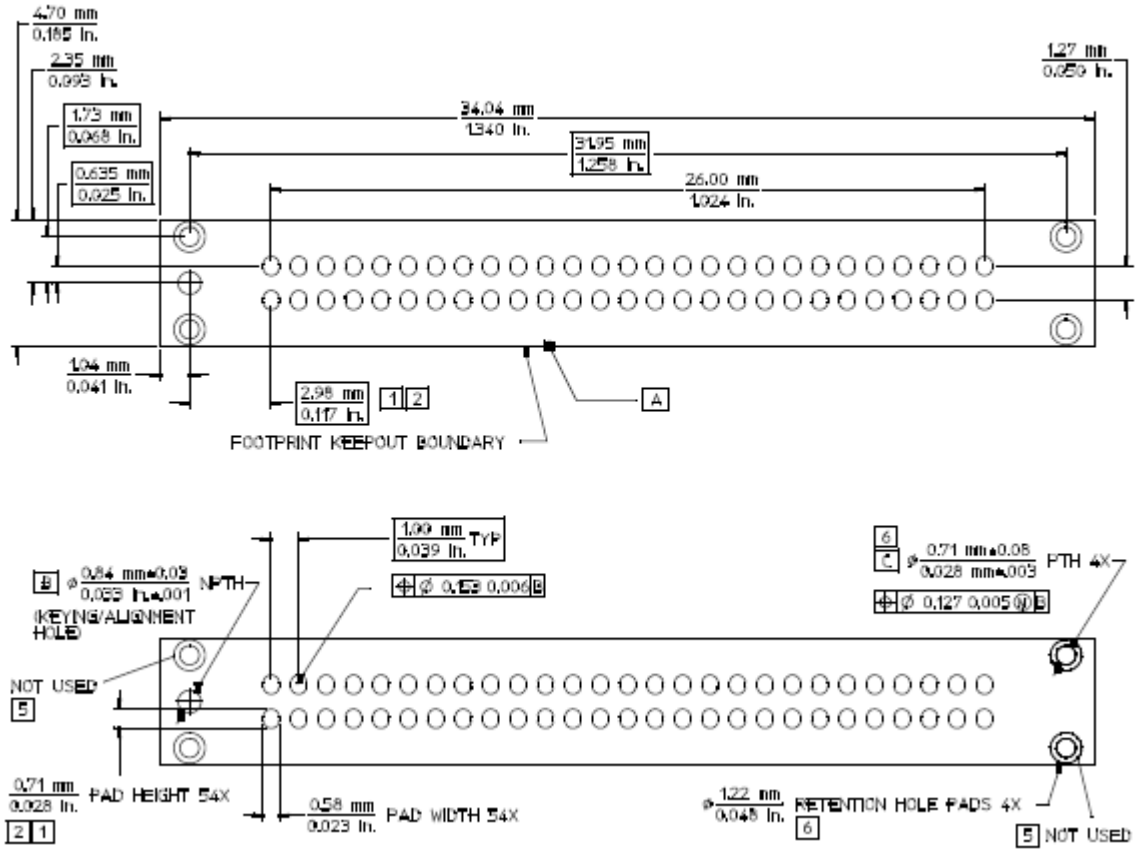


Figure 13 – Mechanical layout for Industry-Standard connectorless probing

Retention module

A retention module (*Figure 14*) is required to provide the mechanical support of the connectorless probe to the target board. The module is simply attached to the board by soldering its legs to the plated through holes that are part of the footprint described above. The probe is then connected to the target by placing the probe head into the retention clip, taking care to maintain polarity, and screwing down the captive fasteners.

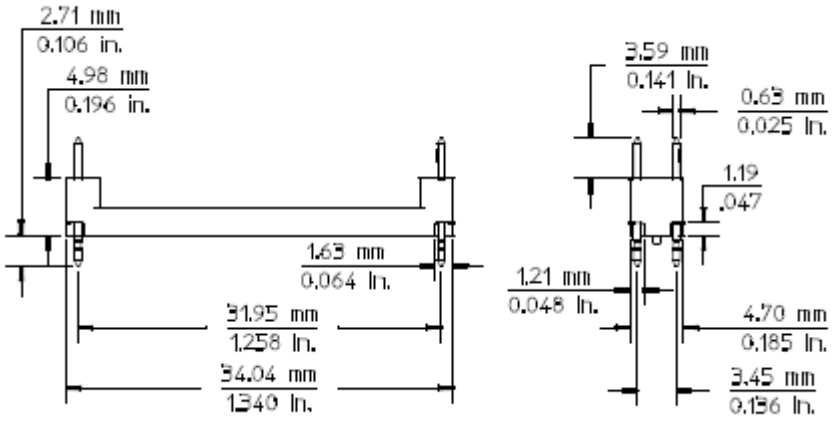
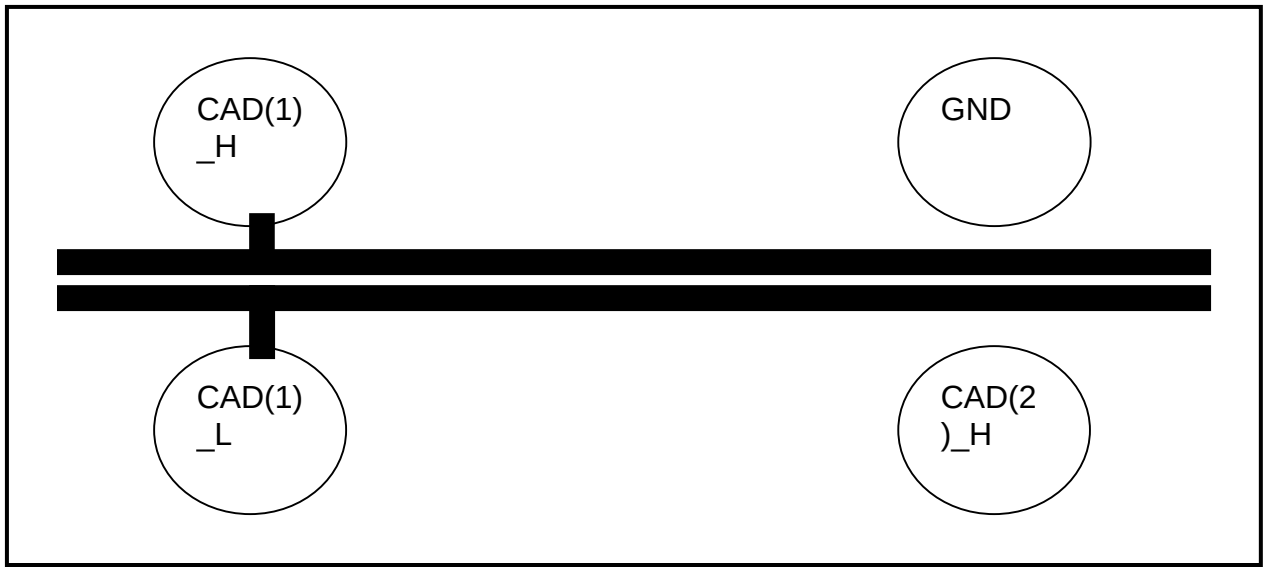


Figure 14 – Mechanical layout for the Industry-Standard connectorless probing retention module

Connectorless probe trace routing – Differential signals in different row, same column

The goal is to minimize the disruption to the standard HT differential pair routing between devices and to minimize any differences in position on the link where each signal is probed, as well as introduce only a minimal and equal length stub to each pad. It is also important to maintain the 5 mil spacing between signals in a pair. The following is an example of a layout for 1 pair where the signals are in the **same column** but **different rows**.

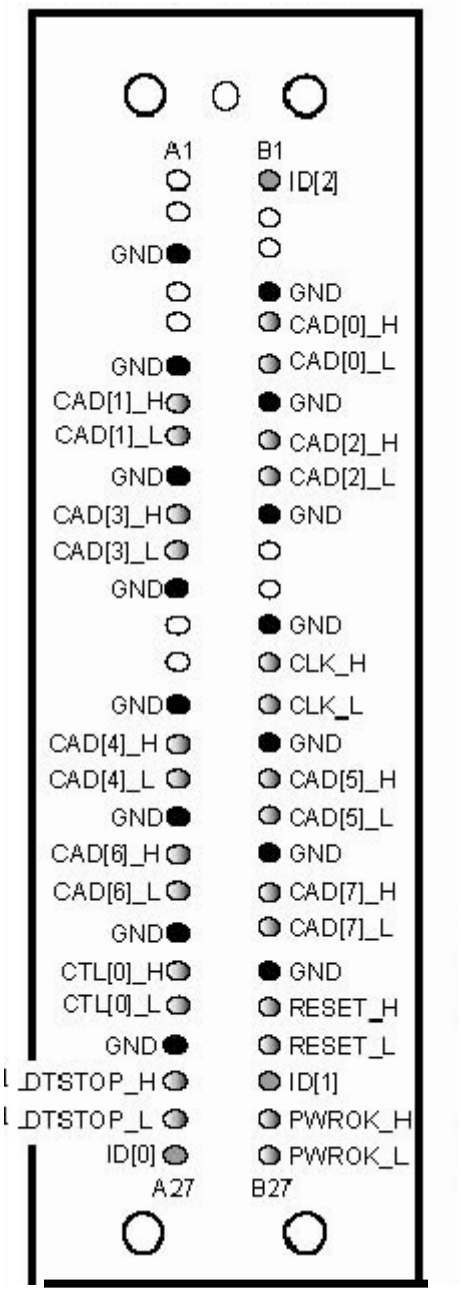


The following pages show a detailed pin out for probing connections required for capturing both Receive and Transmit traffic simultaneously on a 16 bit HT link.

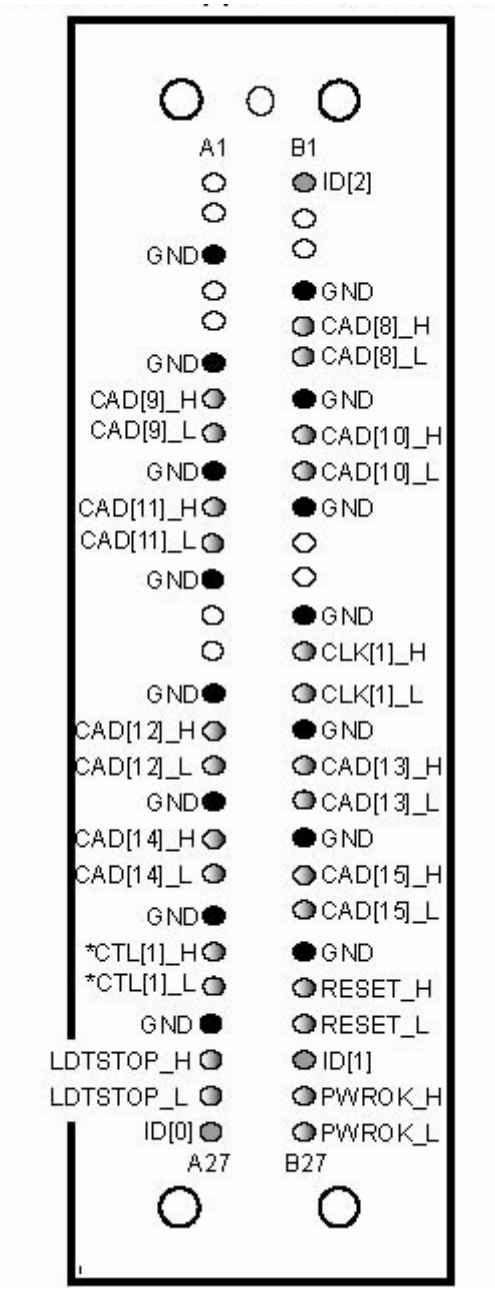
For 8 bit TX and RX data capture use A Lower for TX and B Lower for RX.

For 16 bit TX only, two probing connections are required – A Lower and A Upper.
For 16 bit RX only, two probing connections are required – B Lower and B Upper.

The following diagrams describe certain probing positions as “NO PAD” and others and “NC”. NC indicates the presence of a pad but no connection to circuitry. NO PAD indicates that there is no physical pad on the board. Only pads with signal names need to be created on the board, which may ease trace routing.



A or B Lower



A or B Upper

Sideband signals – The sideband signals can be brought to either the Lower or Upper footprint, but they do not need to be brought to both.

Simulation models and simulation results

By utilizing the SPICE models and simulation, the board designer can observe the behavior of the layout before fabrication. This allows the designer to try variations in trace impedances, lengths, etc. that are sometimes necessary when routing a board. As the results for a typical board show, digital probing has little impact on the HyperTransport link.

7.0 References

HyperTransport I/O Link Specification, Revision 2.00b,
Copyright 2001-2005 HyperTransport Consortium
Available at: http://www.hypertransport.org

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FS2240 Quickstart, FuturePlus Systems, Bedford, NH, www.futureplus.com

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