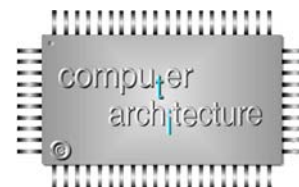


the HTX board

a universal HTX test platform



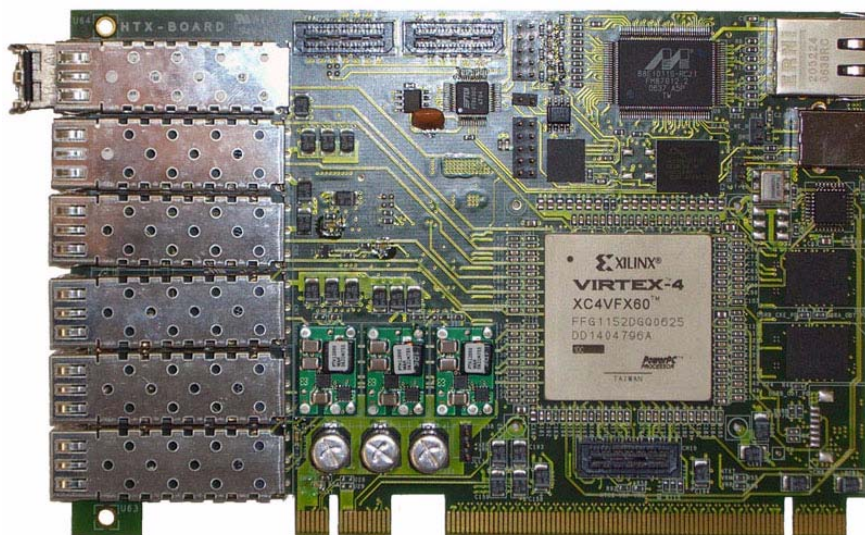
Description

The **HTX-Board** provides a comfortable and efficient way to evaluate user specific devices connected to the HyperTransport™ connector standardized under the name HTX-Connector™. Additionally, the board can be used as high-performance co-processor, communication platform or other custom device requiring low latency and high bandwidth connectivity to the Hypertransport enabled host system.

The HTX-Board with the 16bit wide bi-directional HTX Interface can be plugged to any AMD Opteron™ processor node with HTX, e.g. the Iwill DK8-HTX dual processor Hypertransport-enabled server board. The HT 400MHz DDR interface will deliver 3.2GByte/s bandwidth and a very low latency.

The **HTX-Board** combines the Hypertransport HTX connector with one of the most complex Xilinx FPGAs - a Virtex-4 FX60 as the programmable core logic. The FPGA is surrounded with many useful support chips like DRAMs, user FLASH memory, clock oscillators and drivers.

11 high-speed transceiver channels (multi-gigabit transceivers MGTs) are utilized. Six channels are connected to small form factor pluggable (SFP) sockets, enabling optical physical layer interfaces of various data rates up to 10Gbit/s, delivering an aggregate bandwidth of 15GByte/s. Four channels are connected to a mezzanine connector. The remaining channel is connected to a SATA host connector. The in-system programming infrastructure is kept very flexible. A Xilinx platform FLASH-PROM memory is used



Assembled HTX-Board with Virtex4 FX60

for FPGA configuration after power-on. A JTAG interface is provided for programming the FX60 and the platform PROM. The Xilinx JTAG external adapter can be used for programming and debugging. This interface also supports the Chipscope debugging feature.

Alternatively, an USB1.1 interface can be used for programming the FX60 and the platform PROM from a LINUX-PC. Additionally, this interface establishes a universal communication path to a PC.

A standard Gigabit-Ethernet Phys with RJ45-Connector is connected to the tri-mode Ethernet MAC of the FX60 to support Ethernet communication with the two PowerPCs or the FPGA logic. The dual samtec connectors allow an extension with 4x5 cm mezzanine boards. 21 differential signal pairs are routed from the FPGA to this interface which can also be configured as 42 single ended signals. A 3.3V and 1.8V power supply is available on these pins.

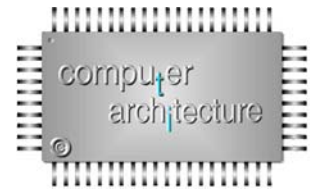
Technical Overview:

- HTX Connector with 16bit LVDS bi-directional interface for HT 400MHz DDR
- FPGA Virtex-4 FX60
- 128MByte of DDR2 DRAM (optional 256MByte)
- 512 Mb of user FLASH, 16bit interface to FPGA
- 125MHz and 200MHz low jitter clock oscillator, jumper selectable
- LVDS clock distribution
- Gigabit Ethernet Interface
- 6 pluggable SFP sockets
- power supply with only 12V and 3.3V from HTX connector
- power consumption of 6 to 24W

The **HTX-Board** can also be used as a stand-alone FPGA design testbed. A complete dual core PowerPC computer system can be programmed into the FPGA. The user FLASH memory can hold the operating system and application software for the embedded cores. The power can be supplied with an off-the-shelf ATX power supply of only 3.3V and 12V.

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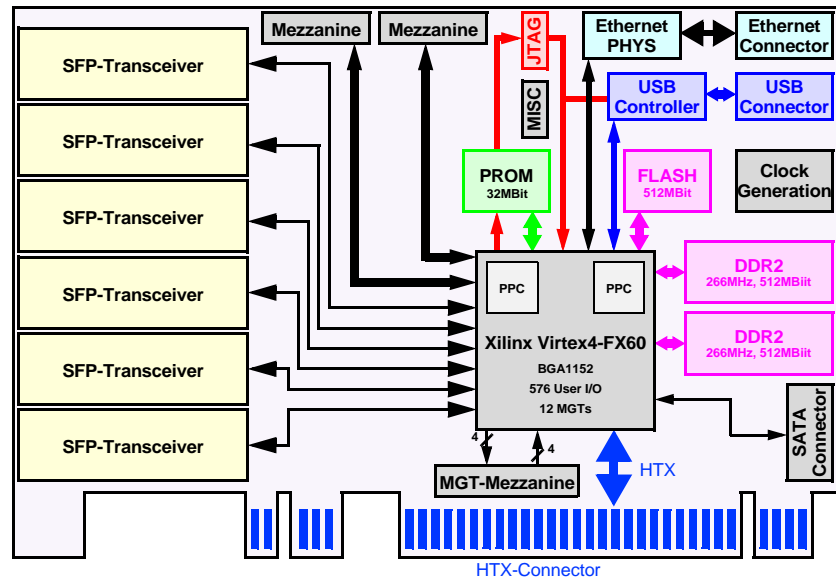


Reconfigurable Logic Device

The Xilinx Virtex4 FPGA FX60 or FX100 in the BGA 1152 ball version can be assembled on the HTX-Board. This chip provides a programmable infrastructure with many features. The Virtex-4 FX provides a high-performance, full-featured solution for embedded platform applications.

FPGA Virtex-4 FX60 features:

- speed grade -10, (-11, -12, on request)
- BGA 1152 with 576 user I/Os
- Flip-Chip Packaging, Pb-Free
- Digital Clock Manager (DCM) blocks
- Additional Phase-Matched Clock Dividers (PMCD)
- Differential Global Clocks
- up to 160 XtremeDSP Slice
 - 18x18, two's complement, signed Multiplier
 - Optional pipeline stages
 - Built-In Accumulator (48-bits) & Adder/Subtractor
- Smart RAM Memory Hierarchy
 - Distributed RAM
 - up to 376 Dual-Port 18-Kbit RAM blocks totaling 6,768 Kb of Memory on chip
 - Optional pipeline stages
 - Optional programmable FIFO logic - Automatically remaps RAM signals as FIFO signals
- High-speed memory interface support: DDR-2 used on board, up to 256 MByte
- 16 RocketIO MultiGigabit Transceivers with SERDES (622Mb/s to 10+Gb/s MGT)
- 2 IBM PowerPC RISC Processor Cores (PPC405 Core with Auxiliary Processor Unit Interface) enabling embedded system solutions



Blockdiagram of the HTX-Board

- Tri-Mode Ethernet MAC
- 90-nm copper CMOS process
- 1.2V core voltage

For more details please refer to the Xilinx Virtex4 FX60/100 user manual.

Assembly options

Many assembly options are possible to support the board as a versatile test platform.

The FPGA FX60 can be replaced by a FX100 providing more internal logic functions. The FPGA available speed grades -10, -11, (-12) can be used.

The 32bit wide DRAM interface (2x 16 bit word width) can be assembled with DDR2 DRAMs of various capacities, starting from 128MB to 256MB.

For the user FLASH memory, a 1Gb, 512Mb, 256Mb or 128Mb device can be assembled.

There are two landing pads for LVDS oscillators which can be selected by the user. Standard frequencies are 125MHz and 200MHz with a very low jitter specification as required for the MGTs. Different LVDS oscillators can be placed on request.

Instead of 3x SFPs a parallel connector for 2 x 68 pin Honda Connectors can be assembled providing 2x 40bit of differential LVDS signal lines. Sufficient ground lines are supplied to control the impedance of the connector and the cable. Compatible cables with various lengths (1-5m) are available on request.

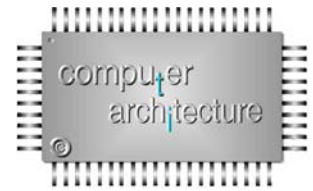
Available Soft-Cores

A constraint file in Xilinx .ucf file format describing the pinout is included.

A HyperTransport core (HT 400MHz DDR, 8bit or 16bit wide) is optionally available.

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FPGA assembly options with features

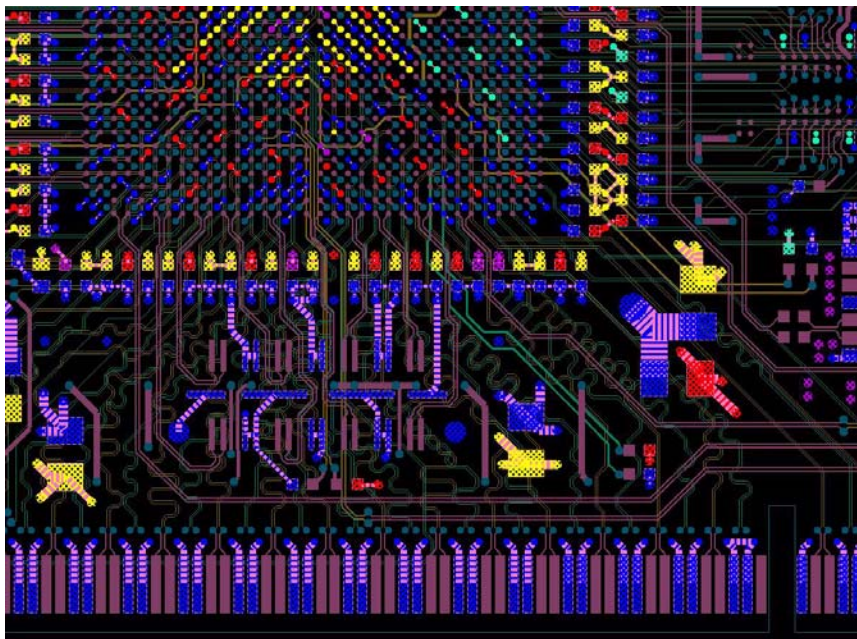
Device	Logic Cells	Block RAM - # of 18Kb Blocks	DCMs	RocketIO Multi Gigabit Tranceivers	Max User I/O
XC4VFX60	56,880	232	12	16 (11 connected)	576
XC4VFX100	94,896	376	12	20 (11 connected)	576

Additional Options

A HTX-Extender board with test pins for LSA connection is available in two versions:

- for the adaption of the HTX signals with differential flying lead probes E5381A from Agilent
- a version with build-in probe interface and direct connection to the Agilent 2x 45 pin 0.05" LSA probe connector

A debug mezzanine board with LEDs, test pins with 0.1" spacing, differential flying probe LSA connector and two SMA coax connectors can be used for further debugging. A layout file in Cadence Allegro format can be supplied to support user specific developments of mezzanine boards.



Layout Section of the HTX-Board

All HTX signal traces on the HTX Board are routed as striplines with controlled impedance and are optimized for equal length, simplifying the HTX interface design. The board is carefully handrouted with only four interconnect layers.

About:

Computer Architecture Group

The Computer Architecture Group at the University of Heidelberg has the expertise to design complex hardware/software systems.

Goals of the applied research activities are to cover a broad range of methodologies for the design of complete high performance systems with the possibility to optimize every level and educate students on the various real world topics.

The group mainly focuses on the design of parallel architectures which achieve their high performance by improving communication between computational devices/units. Scaling such systems is a great challenge to the architecture of the interconnection network (IN) and the network interface controller (NIC). Special attention is paid on the interface between software and hardware to setup communication instructions.

The **HTX-Board** is a development of the University of Heidelberg, Computer Architecture Group.