HyperTransport™ Technology

Interface Design Guide

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HyperTransport technology is a high-speed, high-performance, point-to-point link for integrated circuits, and is designed to meet the bandwidth needs of tomorrow's computing and communications platforms. HyperTransport technology helps reduce the number of buses while providing a high-performance link for PCs, workstations, and servers, as well as numerous embedded applications and highly scalable multiprocessing systems. It is designed to allow chips inside of PCs, networking and communications devices to communicate with each other up to 48 times faster than with some existing bus technologies.

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The HyperTransport Technology Consortium is a nonprofit corporation managed by its members. The consortium promotes the common business interests of providers to the networking, telecommunications, computer and high-performance embedded application through the conduct of a forum for the future development and adoption of the HyperTransport specification.

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Revision History: Interface Design Guide

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Preface

The *HyperTransport™ Technology Interface Design Guide* provides guidelines for designing signal interconnect and power distribution for HyperTransport™ technology systems; including the device, package, and PCB interconnect.

This guide is intended for system, motherboard, chipset, and embedded system designers and other technology professionals interested in the physical implementation details of die, package, and board design in HyperTransport™ technology systems. The reader should be familiar with concepts and terminology presented in both the *HyperTransport™ I/O Link Protocol Specification* and the *HyperTransport™ Technology Electrical Specification*.

To obtain the specifications and information about joining the HyperTransport™ Technology Consortium, please visit the consortium's web site at: http://www.hypertransport.org.

1 Overview

This document provides implementation-specific design examples and design rules that support the example timing budget in the *HyperTransport™ Technology Electrical Specification*. This document assumes the reader is familiar with the *HyperTransport™ I/O Link Protocol Specification* and the *HyperTransport™ Technology Electrical Specification*.

The design guide is divided into two major chapters: Signal Interconnect and Power Distribution. Each chapter addresses the design of the transmitting device package, system board, and receiver device package, as well as pertinent issues affecting both transmitter and receiver silicon.

Throughout the remainder of this document, HyperTransport™ and HyperTransport™ technology are also called HyperTransport, all of which refer to the same technology.

1.1 HyperTransport Signaling Overview

HyperTransport signaling uses low-voltage swing differential signaling with source-synchronous clocking. The transmitted source-synchronous clock is shifted by nominally one-half bit-time in order to facilitate simple data recovery in the receiver. Physical implementation design approaches, rules, and guidelines to maintain the required signal quality and low skew are presented in this document.

1.1.1 General Guidelines

HyperTransport technology consists of groups of signals and an associated clock that make up a clock group.

- All signals within a clock group should be routed nominally alike, so the output timing of the transmitting device matches the input timing of the receiving device.
- All signals in a clock group should experience the same number of layer changes and have the same number of vias.
- Clock group electrical lengths are matched piecewise to meet the timing budget. TX package trace lengths are matched within budget, MB trace lengths are matched within budget, and RX package trace lengths are matched within budget. There are multiple methods by which certain portions of the electrical length of the package can be offset by portions of the system board route in order to compensate for mismatch and still maintain a simple route that meets the skew budget.
- All CAD/CTL/CLK signals are AC-ground-referenced differential pairs referenced to VSS, VDD, or VLDT.
- All CAD/CTL/CLK signals are routed point-to-point. Maintaining signal quality requires impedance matching of the interconnect from device pad to device pad.
- VLDT must be implemented as to achieve a supply impedance that supports the allowed tolerance given the maximum device specific current transient.

1.2 HyperTransport Link Implementations

1.2.1 Common Symmetric Width Implementations

HyperTransport links may be implemented with the same number of CAD wires in either direction. The resulting common symmetric implementations are listed in Table 1.

Table 1. Common Symmetric Width Implementations

Implementation (TX x RX)	Comments
2x2-bit	Link will initialize through hardware to maximum link width available in both directions or, in these cases, 2x2-bit.
4x4-bit	Link will initialize through hardware to maximum link width available in both directions or, in these cases, 4x4-bit.
8x8-bit	Link will initialize through hardware to maximum link width available in both directions (up to 8 bits) or, in these cases, 8x8-bit.
16x16-bit	Link will initialize through hardware to maximum link width available in both directions (up to 8 bits) or, in this case, 8x8-bit.
32x32-bit	Link will initialize through hardware to maximum link width available in both directions (up to 8 bits) or, in this case, 8x8-bit.

1.2.2 Asymmetric Width Implementations

HyperTransport links may alternatively be implemented with different number of CAD wires in either direction. The resulting asymmetric link has the properties and issues listed in Table 2.

Table 2. Asymmetric Width Implementations

Implementation	Comments
2x4, 2x8, 2x16, 2x32	Link will initialize through hardware to maximum link width available in both directions or, in these cases, 2x2-bit.
4x8, 4x16, 4x32	Link will initialize through hardware to maximum link width available in both directions or, in these cases, 4x4-bit.
8x16, 8x32	Link will initialize through hardware to maximum link width available in both directions (up to 8 bits) or, in these cases, 8x8-bit.
16x32	Link will initialize through hardware to maximum link width available in both directions (up to 8 bits) or, this case, 8x8-bit.

1.2.3 HyperTransport Link Frequencies

HyperTransport technology defines six specified frequencies of operation for synchronous clocking mode: 400 million transfers per second (MT/s), 600 MT/s, 800 MT/s, 1000 MT/s, 1200 MT/s, and 1600 MT/s. These frequencies are split into two groups, classified slow and fast, and described in Table 3. Design Guidelines. Some of the electrical characteristics are defined as applicable to slow or fast links to either enable the highest frequency possible or reduce cost.

Table 3. HyperTransport Link Frequencies

Link Frequencies	Group	Effect on Device Characteristics and Design Guidelines
400 MT/s, 600 MT/s, 800 MT/s (or any asynch or pseudo-sync implementation up to and including 800MT/s)	Slow	Input and output edge rates relaxed, input and output pad capacitance increased, link maximum interconnect length extended, proportionally more skew associated with route length mismatches
1000 MT/s, 1200 MT/s, 1600 MT/s (or any asynch or pseudo-sync implementation higher than 800 MT/s)	Fast	Baseline

1.3 Signal Group Definitions

For a given link implementation, HyperTransport links contain the signal groups listed in Table 4, which must be grouped and timed to the associated clock. These group names are referenced throughout this design guideline.

Table 4. Signal Groups for Transfer Timing

Link Width (TX or RX)	Group Names	Signals	Associated Clock
Any	None	PWROK, RESET#	None (asynchronous)
Any	None	LDTSTOP#, LDTREQ#	None (asynchronous)
2-bit (TX)	CAD/CTLOUT	CADOUT[1:0], CTLOUT	CLKOUT
4-bit (TX)	CAD/CTLOUT	CADOUT[3:0], CTLOUT	CLKOUT
8-bit (TX)	CAD/CTLOUT	CADOUT[7:0], CTLOUT	CLKOUT
16-bit (TX)	CAD/CTLOUT_0	CADOUT[7:0], CTLOUT	CLKOUT[0]
	CADOUT_1	CADOUT[15:8]	CLKOUT[1]
32-bit (TX)	CAD/CTLOUT_0	CADOUT[7:0], CTLOUT	CLKOUT[0]
	CADOUT_1	CADOUT[15:8]	CLKOUT[1]
	CADOUT_2	CADOUT[23:16]	CLKOUT[2]
	CADOUT_3	CADOUT[31:24]	CLKOUT[3]
2-bit (RX)	CAD/CTLIN	CADIN[1:0], CTLIN	CLKIN
4-bit (RX)	CAD/CTLIN	CADIN[3:0], CTLIN	CLKIN
8-bit (RX)	CAD/CTLIN	CADIN[7:0], CTLIN	CLKIN
16-bit (RX)	CAD/CTLIN_0	CADIN[7:0], CTLIN	CLKIN[0]
	CADIN_1	CADIN[15:8]	CLKIN[1]
32-bit (RX)	CAD/CTLIN_0	CADIN[7:0], CTLIN	CLKIN[0]
	CADIN_1	CADIN[15:8]	CLKIN[1]
	CADIN_2	CADIN[23:16]	CLKIN[2]
	CADIN_3	CADIN[31:24]	CLKIN[3]

2 Signal Interconnect Design Guide

2.1 Device Physical Interoperability

A look at the route length mismatch and interconnect uncertainties in the *HyperTransport™ Technology Electrical Specification* shows that the physical link must be designed without trace swaps or undue layer crossings. To facilitate this, this design guide defines a standard signal order per link implementation that each HyperTransport device must be able to attain using natural package breakout patterns. This provides a standard for devices to be physically connected with a minimum of route mismatch and undue electrical uncertainties, while providing the device manufacturers the flexibility to choose package types and ballout/pinout patterns to suit their device requirements. Additionally, care should be taken with VLDT in device packages that will be used in minimal layer count boards (two signal layers and two plane layers) so VLDT can be supplied from either physical side of the link. Examples are also provided to show implementations that allow flexibility with VLDT supply distribution.

2.1.1 Required Signal Ordering per System Board Layer

The signal ordering per system board layer is critical to ensuring that HyperTransport devices can be connected to meet the stringent trace-length matching requirements. This design guide defines this signal order per system board layer, progressing clockwise around the periphery of the chip from the top view as the device would be mounted to the system board. This signal ordering is shown in Tables 5 and 6.

Table 5. 16x16-Bit TSM (Top Route Layer)

Distant Device (Top View)																																
CADOUT[0]_H	CADOUT[0]_L	CADOUT[1]_H	CADOUT[1]_L	CADOUT[2]_H	CADOUT[2]_L	CADOUT[3]_H	CADOUT[3]_L	CLKOUT[0]_H	CLKOUT[0]_L	CADOUT[4]_H	CADOUT[4]_L	CADOUT[5]_H	CADOUT[5]_L	CADOUT[6]_H	CADOUT[6]_L	CADOUT[7]_H	CADOUT[7]_L	CTLOUT_H	CTLOUT_L	CTLIN_L	CTLIN_H	CADIN[7]_L	CADIN[7]_H	CADIN[6]_L	CADIN[6]_H	CADIN[5]_L	CADIN[5]_H	CADIN[4]_L	CADIN[4]_H	CLKIN[0]_L	CLKIN[0]_H	CADIN[3]_L	CADIN[3]_H	CADIN[2]_L	CADIN[2]_H	CADIN[1]_L	CADIN[1]_H	CADIN[0]_L	CADIN[0]_H
Local Device																																

Table 6. 16x16-Bit BSM (Bottom Route Layer)

Distant Device (Top View)																															
CADOUT[8]_H	CADOUT[8]_L	CADOUT[9]_H	CADOUT[9]_L	CADOUT[10]_H	CADOUT[10]_L	CADOUT[11]_H	CADOUT[11]_L	CLKOUT[1]_H	CLKOUT[1]_L	CADOUT[12]_H	CADOUT[12]_L	CADOUT[13]_H	CADOUT[13]_L	CADOUT[14]_H	CADOUT[14]_L	CADOUT[15]_H	CADOUT[15]_L	CADIN[15]_L	CADIN[15]_H	CADIN[14]_L	CADIN[14]_H	CADIN[13]_L	CADIN[13]_H	CADIN[12]_L	CADIN[12]_H	CLKIN[1]_L	CLKIN[1]_H	CADIN[11]_L	CADIN[11]_H	CADIN[10]_L	CADIN[10]_H	CADIN[9]_L	CADIN[9]_H	CADIN[8]_L	CADIN[8]_H
Local Device																															

2.1.2 Recommended Package Ballouts/Pinouts

Recommended device package ballouts are shown as examples and to illustrate an added benefit achievable when connecting two of the same devices together or two devices using these example ballouts, as described in Section 2.3.1.

2.2 Device Design Guidelines

A basic view of an example device bump pattern is given to show an implementation that supports the package recommendations and design rules included in this design guide.

2.2.1 Example I/O Pad Configuration

The bump configuration shown in Figure 1 is provided only to show an example that supports the electrical design rules and the recommended package ballout/pinout.

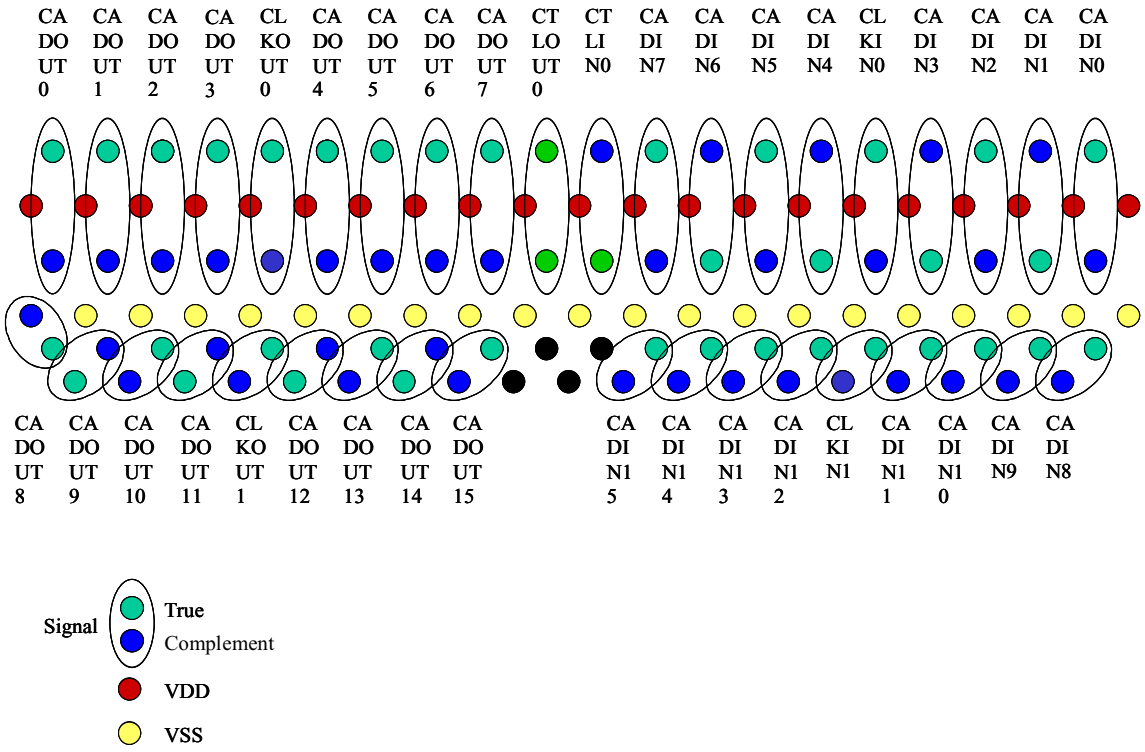


Figure 1. Example I/O Pad Configuration

2.2.1.1 I/O Pad Capacitance

The *HyperTransport™ Technology Electrical Specification* requires input and output pad capacitance (including all circuits and parasitic capacitance associated with the pad) to be limited. This is critical in attaining the signal performance required specifically for links above 800 MT/s.

2.2.1.2 ATE Test Load Circuits Versus System Reference Load

System reference loads shown in the *HyperTransport™ Technology Electrical Specification* mimic a worst-case system reference load for outputs. This load circuit is defined to roughly match the resulting load from the system board design rules described in Section 2.4.

2.3 Device Package Design Guidelines

2.3.1 Package Signal Ballout/Pinout Recommendations

2.3.1.1 16x16-Bit High-Speed (>800 MT/s) Link

The ballout shown in Table 7 is recommended for devices implementing 16x16-bit fast links. This ballout allows natural breakout patterns to achieve the recommended signal ordering on each layer. Additionally,

using this ballout on both the local and the distant devices allows the natural mismatch of the system board trace (due the package pitch) to be compensated by the package trace mismatch. The result is a very low skew route between local and distant devices without the need for excessive length matching.

Table 7. 16x16-Bit High-Speed Link Recommended Ballout/Pinout

4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row
CADOUT_H[9]	CADOUT_H[8]	CADOUT_L[8]	VSS	CADOUT_H[0]
CADOUT_L[9]	VDD	CADOUT_L[1]	CADOUT_H[1]	CADOUT_L[0]
CADOUT_H[11]	CADOUT_H[10]	CADOUT_L[10]	VDD	CADOUT_H[2]
CADOUT_L[11]	VSS	CADOUT_L[3]	CADOUT_H[3]	CADOUT_L[2]
CADOUT_H[12]	CLKOUT_H[1]	CLKOUT_L[1]	VSS	CLKOUT_H[0]
CADOUT_L[12]	VDD	CADOUT_L[4]	CADOUT_H[4]	CLKOUT_L[0]
CADOUT_H[14]	CADOUT_H[13]	CADOUT_L[13]	VDD	CADOUT_H[5]
CADOUT_L[14]	VSS	CADOUT_L[6]	CADOUT_H[6]	CADOUT_L[5]
FREE	CADOUT_H[15]	CADOUT_L[15]	VSS	CADOUT_H[7]
FREE	VDD	CTLOUT_L	CTLOUT_H	CADOUT_L[7]
CADIN_L[15]	FREE	FREE	VDD	CTLIN_L
CADIN_H[15]	VSS	CADIN_H[7]	CADIN_L[7]	CTLIN_H
CADIN_L[13]	CADIN_L[14]	CADIN_H[14]	VSS	CADIN_L[6]
CADIN_H[13]	VDD	CADIN_H[5]	CADIN_L[5]	CADIN_H[6]
CLKIN_L[1]	CADIN_L[12]	CADIN_H[12]	VDD	CADIN_L[4]
CLKIN_H[1]	VSS	CLKIN_H[0]	CLKIN_L[0]	CADIN_H[4]
CADIN_L[10]	CADIN_L[11]	CADIN_H[11]	VSS	CADIN_L[3]
CADIN_H[10]	VDD	CADIN_H[2]	CADIN_L[2]	CADIN_H[3]
CADIN_L[8]	CADIN_L[9]	CADIN_H[9]	VDD	CADIN_L[1]
CADIN_H[8]	VSS	CADIN_H[0]	CADIN_L[0]	CADIN_H[1]
4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row

Edge of Package (Top View)

2.3.1.2 8x8-Bit High-Speed (>800 MT/s) Link

Table 8. 8x8-Bit High-Speed Link Recommended Ballout/Pinout

4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row
FREE	FREE	FREE	VSS	CADOUT_H[0]
FREE	VDD	CADOUT_L[1]	CADOUT_H[1]	CADOUT_L[0]
FREE	FREE	FREE	VDD	CADOUT_H[2]
FREE	VSS	CADOUT_L[3]	CADOUT_H[3]	CADOUT_L[2]
FREE	FREE	FREE	VSS	CLKOUT_H
FREE	VDD	CADOUT_L[4]	CADOUT_H[4]	CLKOUT_L
FREE	FREE	FREE	VDD	CADOUT_H[5]
FREE	VSS	CADOUT_L[6]	CADOUT_H[6]	CADOUT_L[5]
FREE	FREE	FREE	VSS	CADOUT_H[7]
FREE	VDD	CTLOUT_L	CTLOUT_H	CADOUT_L[7]
FREE	FREE	FREE	VDD	CTLIN_L
FREE	VSS	CADIN_H[7]	CADIN_L[7]	CTLIN_H
FREE	FREE	FREE	VSS	CADIN_L[6]
FREE	VDD	CADIN_H[5]	CADIN_L[5]	CADIN_H[6]
FREE	FREE	FREE	VDD	CADIN_L[4]
FREE	VSS	CLKIN_H	CLKIN_L	CADIN_H[4]
FREE	FREE	FREE	VSS	CADIN_L[3]
FREE	VDD	CADIN_H[2]	CADIN_L[2]	CADIN_H[3]
FREE	FREE	FREE	VDD	CADIN_L[1]
FREE	VSS	CADIN_H[0]	CADIN_L[0]	CADIN_H[1]
4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row

Edge of Package (Top View)

2.3.1.3 8x8-Bit Low-Speed (≤800 MT/s) Link

Table 9. 8x8-Bit Low-Speed Link Recommended Ballout/Pinout

4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row
FREE	FREE	FREE	VSS	CADOUT_H[0]
FREE	VDD	CADOUT_L[1]	CADOUT_H[1]	CADOUT_L[0]
CADOUT_H[5]	CADOUT_H[4]	CADOUT_L[4]	VDD	CADOUT_H[2]
CADOUT_L[5]	VSS	CADOUT_L[3]	CADOUT_H[3]	CADOUT_L[2]
CADOUT_H[7]	CADOUT_H[6]	CADOUT_L[6]	VSS	CLKOUT_H[0]
CADOUT_L[7]	VDD	CTLOUT_L	CTLOUT_H	CLKOUT_L[0]
CADIN_L[6]	CADIN_L[7]	CADIN_H[7]	VDD	CTLIN_L
CADIN_H[6]	VSS	CLKIN_H[0]	CLKIN_L[0]	CTLIN_H
CADIN_L[4]	CADIN_L[5]	CADIN_H[5]	VSS	CADIN_L[3]
CADIN_H[4]	VDD	CADIN_H[2]	CADIN_L[2]	CADIN_H[3]
FREE	FREE	FREE	VDD	CADIN_L[1]
FREE	VSS	CADIN_H[0]	CADIN_L[0]	CADIN_H[1]
4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row

Edge of Package (Top View)

2.3.1.4 Considerations for Pin and Socket Signal Crosstalk

These pinouts do not and cannot define what signals will be used on FREE signal balls or pins. However, caution must be used when assigning these locations to prevent significant differential and common mode noise on any of the HyperTransport signals due to crosstalk from coupled signals in the pins or pin sockets.

The following types of signals are discouraged from being placed on pins marked FREE:

- Signals that may act as significant aggressors with edges faster than 2 V/ns and current transients of greater than 30 mA/ns.
- Large voltage swing, single-ended interfaces (>1.8 V) adjacent to HyperTransport links should be shielded by a row of VSS, VDD, or VLDT pins.

Signals that are good candidates to be placed in the pinout on pins marked FREE:

- DC power supply pins
- Static signal pins
- Signals that will not act as significant aggressors.

Ideally, the HyperTransport signals would be surrounded by VDD/VLDT, or VSS pins such that no switching signal could be a significant aggressor. In the worst case, the number of aggressors on each HyperTransport signal should be minimized such that each signal is coupled to more AC return pins (VDD/VLDT, or VSS) than it is to signals that do not use HyperTransport technology.

2.3.2 VLDT Supply Ballout/Pinout Recommendations

The purpose of this section is to introduce VLDT ballout/pinout approaches in conjunction with the signal ballout/pinout recommendations. Using the high-speed 16x16-bit recommended ballout shown in Table 7, two different general approaches for VLDT balls/pins are shown in Tables 10 and 11. More detail on system design guidelines for VLDT generation, distribution, and decoupling can be found in Chapter 3.

The approach illustrated in Table 10 allows VLDT to be connected to both sides or to a single side, providing the package design provides sufficient metallization to connect the pins on either physical side of the link together. The VLDT connection to the system board can be made on the same layer as one on which the HyperTransport signals are routed.

The approach shown in Table 11 uses significantly more ball/pin resources in the package to allow VLDT to be connected to all balls/pins if a dedicated plane layer in the system board can be used for VLDT distribution. Careful device package design can also allow this approach to be used on low layer count boards by using the same package metallization as shown in Table 11.

Table 10. VLDT Ballout for Minimal Layer Count Systems

4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row
		VLDT	VSS	VLDT
	VLDT	VSS	VLDT	VSS
VLDT	VSS	VLDT	VSS	VLDT
VSS	VDLT	VSS	VLDT	VSS
CADOUT_H[9]	CADOUT_H[8]	CADOUT_L[8]	VSS	CADOUT_H[0]
CADOUT_L[9]	VDD	CADOUT_L[1]	CADOUT_H[1]	CADOUT_L[0]
CADOUT_H[11]	CADOUT_H[10]	CADOUT_L[10]	VDD	CADOUT_H[2]
CADOUT_L[11]	VSS	CADOUT_L[3]	CADOUT_H[3]	CADOUT_L[2]
CADOUT_H[12]	CLKOUT_H[1]	CLKOUT_L[1]	VSS	CLKOUT_H[0]
CADOUT_L[12]	VDD	CADOUT_L[4]	CADOUT_H[4]	CLKOUT_L[0]
CADOUT_H[14]	CADOUT_H[13]	CADOUT_L[13]	VDD	CADOUT_H[5]
CADOUT_L[14]	VSS	CADOUT_L[6]	CADOUT_H[6]	CADOUT_L[5]
FREE	CADOUT_H[15]	CADOUT_L[15]	VSS	CADOUT_H[7]
FREE	VDD	CTLOUT_L	CTLOUT_H	CADOUT_L[7]
CADIN_L[15]	FREE	FREE	VDD	CTLIN_L
CADIN_H[15]	VSS	CADIN_H[7]	CADIN_L[7]	CTLIN_H
CADIN_L[13]	CADIN_L[14]	CADIN_H[14]	VSS	CADIN_L[6]
CADIN_H[13]	VDD	CADIN_H[5]	CADIN_L[5]	CADIN_H[6]
CLKIN_L[1]	CADIN_L[12]	CADIN_H[12]	VDD	CADIN_L[4]
CLKIN_H[1]	VSS	CLKIN_H[0]	CLKIN_L[0]	CADIN_H[4]
CADIN_L[10]	CADIN_L[11]	CADIN_H[11]	VSS	CADIN_L[3]
CADIN_H[10]	VDD	CADIN_H[2]	CADIN_L[2]	CADIN_H[3]
CADIN_L[8]	CADIN_L[9]	CADIN_H[9]	VDD	CADIN_L[1]
CADIN_H[8]	VSS	CADIN_H[0]	CADIN_L[0]	CADIN_H[1]
VSS	VLDT	VSS	VLDT	VSS
VLDT	VSS	VLDT	VSS	VLDT
	VLDT	VSS	VLDT	VSS
		VLDT	VSS	VLDT
4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row

Edge of Package (Top View)

Table 11. VLDT Ballout for Deeper Layer Count Systems

6th Row	5th Row	4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row
				VLDT	VSS	VLDT
			VLDT	VSS	VLDT	VSS
		VLDT	VSS	VLDT	VSS	VLDT
		VSS	VDLT	VSS	VLDT	VSS
		CADOUT_H[9]	CADOUT_H[8]	CADOUT_L[8]	VSS	CADOUT_H[0]
		CADOUT_L[9]	VDD	CADOUT_L[1]	CADOUT_H[1]	CADOUT_L[0]
		CADOUT_H[11]	CADOUT_H[10]	CADOUT_L[10]	VDD	CADOUT_H[2]
		CADOUT_L[11]	VSS	CADOUT_L[3]	CADOUT_H[3]	CADOUT_L[2]
		CADOUT_H[12]	CLKOUT_H[1]	CLKOUT_L[1]	VSS	CLKOUT_H[0]
VSS	VLDT	CADOUT_L[12]	VDD	CADOUT_L[4]	CADOUT_H[4]	CLKOUT_L[0]
VLDT	VSS	CADOUT_H[14]	CADOUT_H[13]	CADOUT_L[13]	VDD	CADOUT_H[5]
VSS	VLDT	CADOUT_L[14]	VSS	CADOUT_L[6]	CADOUT_H[6]	CADOUT_L[5]
VLDT	VSS	FREE	CADOUT_H[15]	CADOUT_L[15]	VSS	CADOUT_H[7]
VSS	VLDT	FREE	VDD	CTLOUT_L	CTLOUT_H	CADOUT_L[7]
VLDT	VSS	CADIN_L[15]	FREE	FREE	VDD	CTLIN_L
VSS	VLDT	CADIN_H[15]	VSS	CADIN_H[7]	CADIN_L[7]	CTLIN_H]
VLDT	VSS	CADIN_L[13]	CADIN_L[14]	CADIN_H[14]	VSS	CADIN_L[6]
VSS	VLDT	CADIN_H[13]	VDD	CADIN_H[5]	CADIN_L[5]	CADIN_H[6]
VLDT	VSS	CLKIN_L[1]	CADIN_L[12]	CADIN_H[12]	VDD	CADIN_L[4]
		CLKIN_H[1]	VSS	CLKIN_H[0]	CLKIN_L[0]	CADIN_H[4]
		CADIN_L[10]	CADIN_L[11]	CADIN_H[11]	VSS	CADIN_L[3]
		CADIN_H[10]	VDD	CADIN_H[2]	CADIN_L[2]	CADIN_H[3]
		CADIN_L[8]	CADIN_L[9]	CADIN_H[9]	VDD	CADIN_L[1]
		CADIN_H[8]	VSS	CADIN_H[0]	CADIN_L[0]	CADIN_H[1]
		VSS	VDLT	VSS	VLDT	VSS
		VLDT	VSS	VLDT	VSS	VLDT
			VLDT	VSS	VLDT	VSS
				VLDT	VSS	VLDT
6th Row	5th Row	4th Inner Row	3rd Inner Row	2nd Inner Row	1st Inner Row	Outer Row

Edge of Package (Top View)

2.3.3 Package Layer Stackup Guidelines

HyperTransport devices can be packaged using a number of technologies, each having a wide variety of layer counts and applicable physical design rules. Organic and ceramic ball grid arrays (BGA) are expected to be the primary package types of choice. Flip-chip die attachment is recommended over wirebonded die attachment for all but the lowest link frequencies due to the reduced inductance in both

signal and power distribution paths. Wirebonded packaging is recommended only for devices implementing 400-MT/s links. The recommended layer stackup drawings (Figures 2, 3, 4, and 5) show minimum physical design rules that may be employed for short distances during bump escape routing.

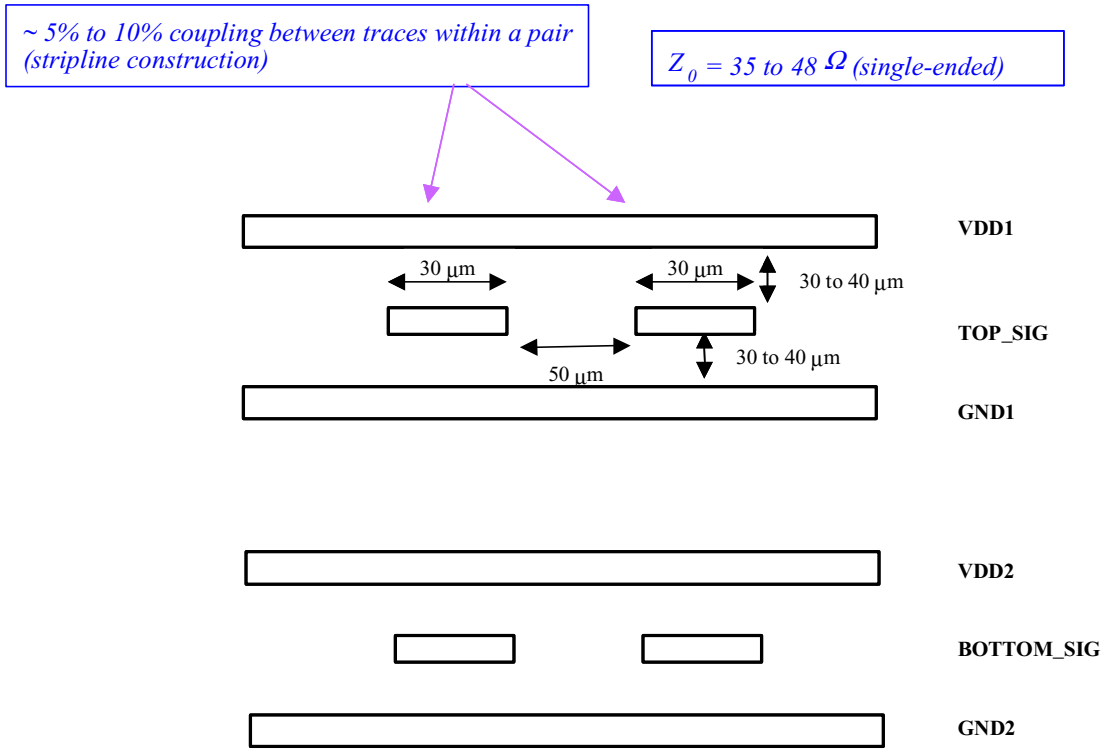


Figure 2. Possible 2-2-2 Organic Flip-Chip Package Stackup (Stripline Traces)

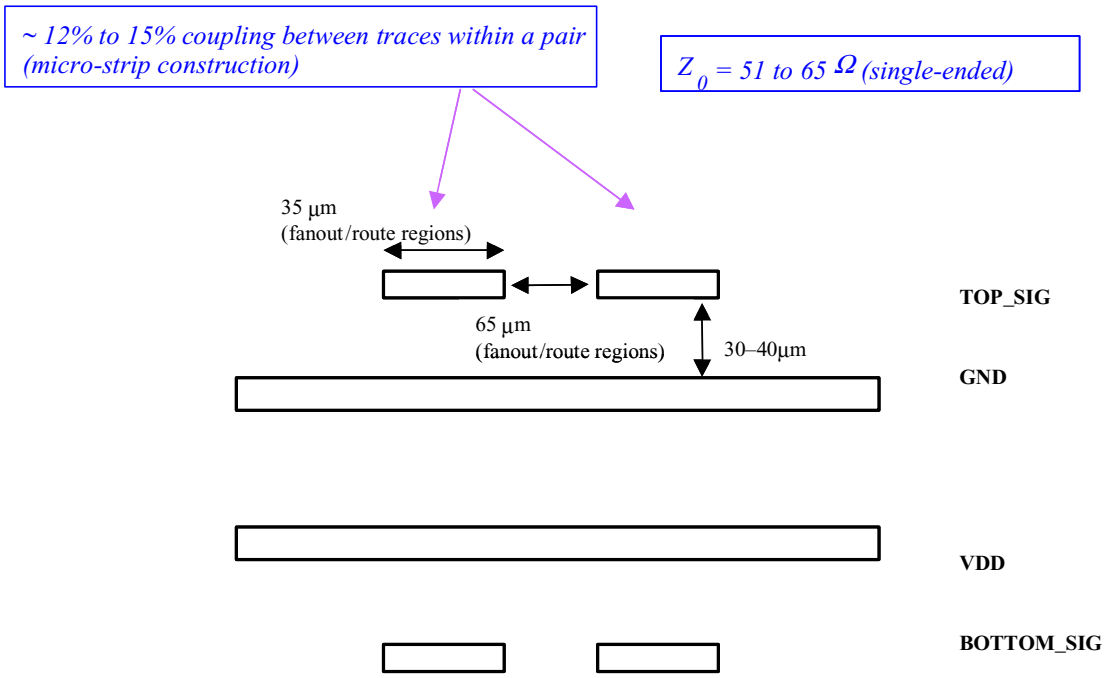


Figure 3. Possible 1-2-1 Organic Flip-Chip Package Stackup (Micro-Strip Traces)

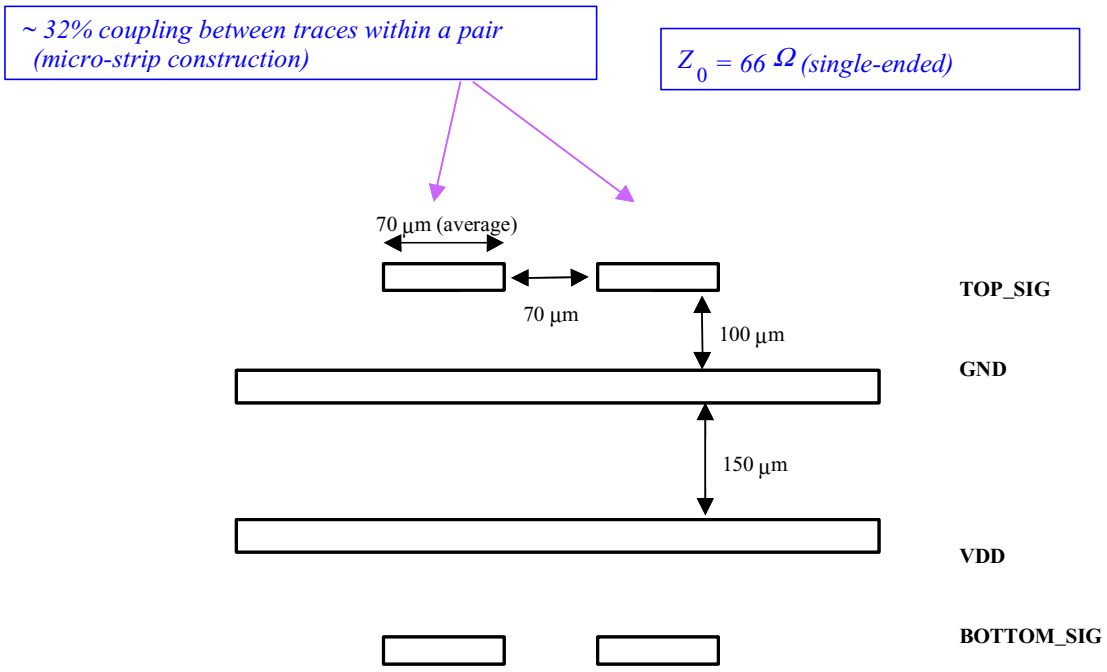


Figure 4. Possible Organic Wirebond Package Stackup (Micro-Strip Traces)

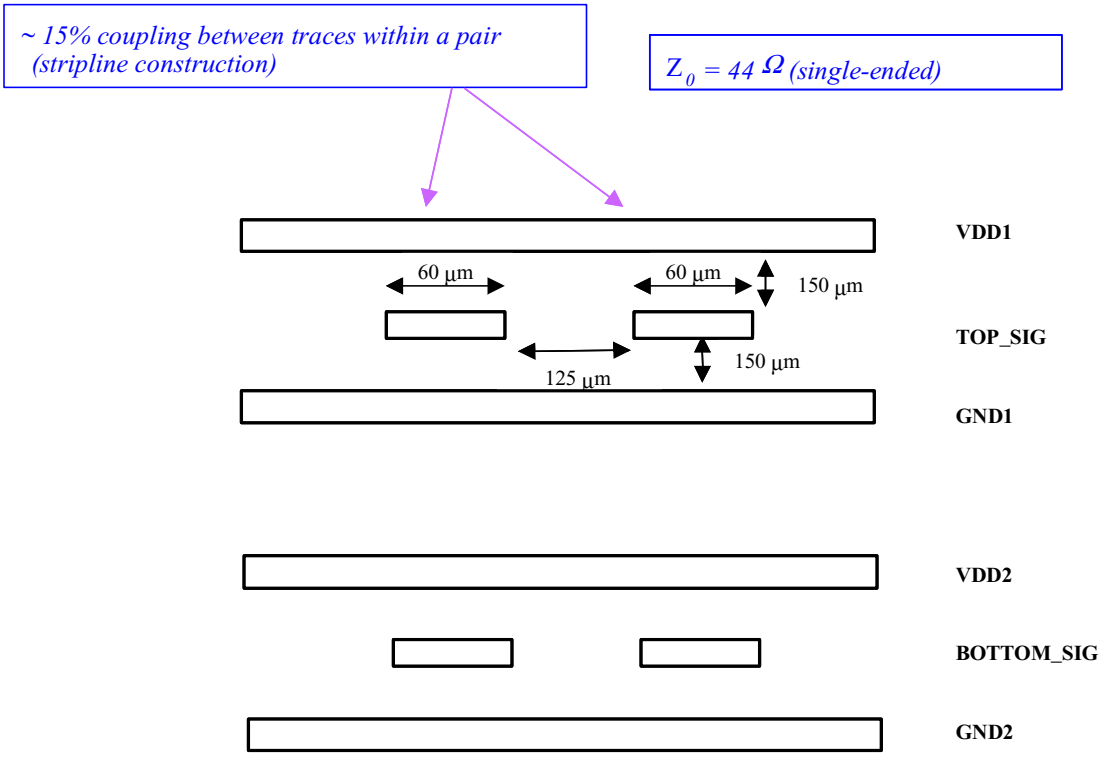


Figure 5. Possible Ceramic Flip-Chip Package Stackup (Stripline Traces)

2.3.4 Package Trace Electrical Specification

For either organic/copper or ceramic/tungsten (molybdenum) packages, the ideal nominal targets for trace characteristic impedance to match the system board trace characteristics impedance are as follows:

- Z_{OD} = 100 Ω target (differential impedance)
- Z_O = 60 Ω target (single-ended impedance)

However, stripline constructions will typically give values smaller than this (around 35–65 Ω) in both organic and ceramic packages. These design guidelines provide recommendations with adjusted trace spacing in certain areas of the trace routes that attempt to achieve the following:

- Z_{OD} as close to 100 Ω as practical
- Minimized trace crosstalk

As a practical approach to meeting these goals, this design guide defines first trace width and intra-pair spacing rules that given a package technology and stackup works to approach the 100 Ω differential impedance. The guide then defines the pair-to-pair pitch such that the intra-pair coupling is sufficiently stronger than the inter-pair coupling, so that pair-to-pair crosstalk is minimized.

2.3.4.1 Organic/Copper Package Trace Electrical Specifications

- Maximum R_{DC} = 3.4 Ω/inch
- Maximum R_{AC} = 5.3 Ω/inch @1 GHz
- Maximum G_{AC} = 0.32 S/inch @1 GHz
- T_{PD} = 150–170 ps/inch (single-ended) depending upon stripline versus micro-strip construction, actual dielectric material, and manufacturing variations.

2.3.4.2 Ceramic/Tungsten (Molybdenum) Package Trace Electrical Specifications

- Maximum R_{DC} = 4.2 Ω/inch
- Maximum R_{AC} = 7.0 Ω/inch @1 GHz
- Maximum G_{AC} = 0.1 S/inch @1 GHz
- T_{PD} = 270 ps/inch (single-ended)

2.3.5 Package Trace Routing Guidelines

Packages for HyperTransport devices must consider both timing uncertainty and signal integrity of the signals on the substrate and at the interface to both the die and the system board. To maintain signal integrity of the signal propagating on the package, the package designer must do the following:

- Control the trace Z_O and Z_{OD} using both trace width and spacing and by defining the package layer stackup.
- Control crosstalk by maximizing spacing between distinct differential pairs.
- Avoid on-package trace impedance discontinuities due to traces routed over reference plane voids.
- Minimize inductive effects in both signals and power distribution by limiting the length of wirebonds and maximizing the spacing between wirebonds (recommended for 400 MT/s links only).

Table 12. Summary of Package Design Rules

Description		Definition/Parameter[1]	Rules[2]			
			Link Speed	**Organic Micro-Strip[3]**	**Organic Stripline[4]**	**Ceramic Stripline[5]**
1a	_H to _L trace length matching (differential skew) using trace-by-trace compensation	Defines the absolute length difference allowed between _H and _L signal traces. Parameter=Diffpkgskew 400–800 MT/s = 20 ps >800 MT/s = 10 ps	400–800 MT/s	3300 µm	2900 µm	1800 µm
			>800 MT/s	1600	1450	900
1b	_H to _L trace length matching (differential skew) using zero mismatch boundaries	Defines the absolute length difference allowed between _H and _L signal traces. Parameter=Diffpkgskew 400–800 MT/s = 20 ps >800 MT/s = 10 ps	400–800 MT/s	3300	2900	1800
			>800 MT/s	1600	1450	900
1c	_H to _L trace length matching (differential skew) using naturally compensating matching[6]	Defines the absolute length difference allowed between _H and _L signal traces. For perpendicularly oriented package pins, the target trace mismatch is equal to the pin pitch with positive tolerance to limit the maximum trace mismatch or negative tolerance to limit the minimum trace mismatch. Parameter = Diffpkgskew 400–800 MT/s = 20 ps >800 MT/s = 10 ps	400–800 MT/s: Parallel Perpendicular	3300 pitch +/- 3300	2900 pitch+/-2900	1800 pitch +/- 1800
			>800 MT/s: Parallel Perpendicular	1600 pitch +/- 1600	1450 pitch+/-1450	900 pitch +/- 900
2	CLK to CAD/CTL trace length matching (CLK centering) – this is the most difficult rule to achieve	Defines the length difference allowed between the longest or shortest average of _H and _L for any CAD/CTL signal within a clock group and the average length of _H and _L for the associated CLK. Parameter = TPKGskew/RPKGskew	400 MT/s	8300	7400	4700
			600 MT/s	6600	5900	3700
			800 MT/s	4100	3700	2300
			1000 MT/s	3300	2950	1800
			1200 MT/s	2100	1900	1200
			1600 MT/s	1600	1450	900

Description		Definition/Parameter[1]	Rules[2]			
3	CAD/CTL to CAD/CTL trace length matching	Defines the length difference allowed between the longest and shortest average of _H and _L for all CAD/CTL signals within a clock group. Parameter = TPKGskewcad/ RPKGskewcad[7]	400 MT/s	16600	14800	9400
			600 MT/s	13200	11800	7400
			800 MT/s	8200	7400	4600
			1000 MT/s	6600	5900	3600
			1200 MT/s	4200	3800	2400
			1600 MT/s	3200	2900	1800
4	CAD/CTL group to CAD/CTL group[8]	Defines the length difference allowed between the longest or shortest average of _H and _L of one transmit or receive clock group to the shortest or longest average of _H and _L to any other transmit or receive clock group. Note that there is no requirement to match a transmit clock group to a receive clock group. Parameter=Rclk2Rclkskew (divided equally between system board and packages, therefore each package = 250 ps).	Any	41600	37300	23500

Notes:

1. *Parameter references are to the detailed transfer timing budget found in appendices K and L of the* HyperTransport™ I/O Link Specification*, Rev. 1.03.*
2. *Units are in μm.*
3. *Propagation rate used for organic micro-strip is 6.7 ps/mm.*
4. *Propagation rate used for organic stripline is 6.0 ps/mm.*
5. *Propagation rate used for ceramic stripline is 10.6 ps/mm.*
6. *Relative lengths of _H and _L between the package and the motherboard need to reverse to achieve the length compensation. For example, if _H trace is shorter than _L trace on the package, then _H trace must be longer on the motherboard than _L trace.*
7. *TPKGskewcad and RPKGskewcad are merely 2 times the TPKGskew and RPKGskew allowed, and therefore if these rules are met, TPKGskewcad and RPKGskewcad are met also.*
8. *CAD-group-to-CAD-group mismatches allowances are extreme not-to-exceed numbers. Good design should easily maintain mismatch significantly lower than these maximums.*

2.3.6 Trace-Length Mismatch Control

There are three primary methods that may be used for controlling the trace electrical length mismatch in HyperTransport systems:

- Trace-by-trace compensated matching
- Zero mismatch boundaries
- Naturally compensating matching

It is the responsibility of the device vendor to choose which method provides the best performance and requires the correct amount of design in support for their market.

This design guideline recommends the naturally compensating matching method combined with the strongly recommended signal breakout ordering and the recommended ballouts shown earlier. This provides a highly skew-controlled physical implementation that is simple and straightforward to design into highly cost-effective system boards.

2.3.6.1 Trace-by-Trace Compensated Matching

Trace-by-trace compensation is the most general and the most complicated of the methods. In this method, the transmitter package and receiver trace lengths for all traces must be known and the system board must then be routed to compensate for the combined mismatch between true and complement and within CLK groups.

2.3.6.2 Zero Mismatch Boundaries

Zero mismatch boundaries are defined points along the trace of each signal where the package trace length and the system board length combine to a defined electrical length. Traces on the system board can then be simply matched between these points. These zero mismatch boundaries can be defined on either the system board (where package electrical length plus system board electrical length equals the defined electrical length) or at the package ball/pin such that the package traces are matched, thus requiring the system board traces to be matched.

2.3.6.3 Naturally Compensating Matching

Naturally compensating matching, shown in Figure 6, requires that the transmitter and receiver be physically designed such that the package traces are routed to lengths either matched or mismatched based upon the device ballout/pinout.

If, for example, a true and a complement signal are placed on pins parallel to the package edge, then the package trace lengths would be matched. In this case, the resulting system board trace lengths would naturally have no natural mismatch due to the package breakout routing.

However, if a true and a complement signal are placed on pins perpendicular to the package edge, then the package trace lengths would be mismatched by one package-pin pitch. The natural package breakout routing would also be mismatched by one package-pin pitch. Electrically, this creates a zero mismatch boundary at the package edge without artificially creating a point at which the lengths must be checked or requiring *swizzle* routing to match the lengths. This method does also have an error associated with the

electrical length of the trace on the package not quite matching the electrical length of the trace on the system board. The recommended ballouts included in these design guidelines support this type of trace length matching.

LENGTH_TRUE + 50 mils = LENGTH_COMPLEMENT (on motherboard)

LENGTH_TRUE – 1270 µm = LENGTH_COMPLEMENT (on package substrate)

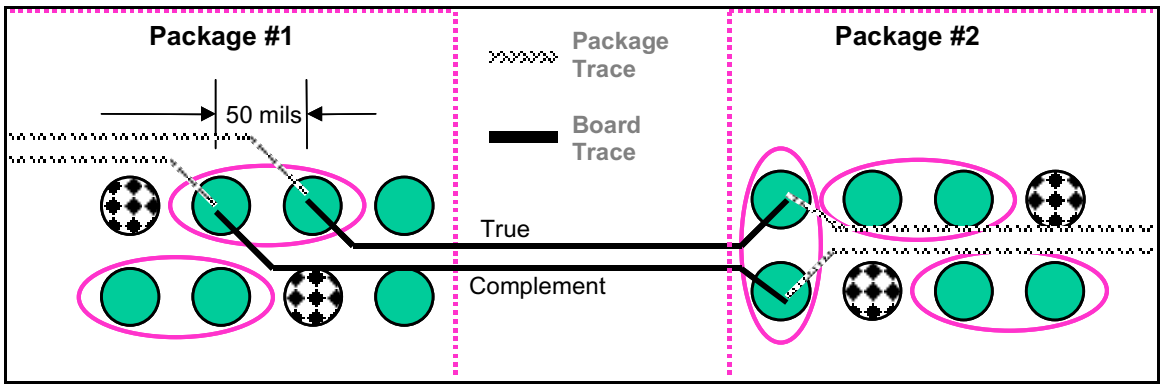


Figure 6. Naturally Compensating Trace Length Matching

2.3.7 Package Routing Rules for Individual Signal Groups

The package routing rules are defined per signal group for two distinct areas of the package trace route. The areas of the package trace route are defined as follows:

- *Escape*—This area uses minimum physical design rules to escape the bumps for the smallest length possible. Electrical trace specifications in this area are not optimal.
- *Fanout*—This area uses physical design rules that are closer to meeting the electrical trace specifications, while physically fanning out from the escape region.
- *Route*—This area uses physical design rules that meet (or get as close as practical to) the electrical trace specifications. Routes at these physical rules are used to complete the connections to the balls/pins.

2.3.7.1 CAD/CAD# and CTL/CTL#

Differential Routing Rules

Each trace within the differential pair is routed on the same layer and has the same number of vias. Trace length within the pair is measured absolutely.

Pair Routing Rules

CAD/CAD# and CTL/CTL# within a clock group should be treated identically. Each signal is routed as a differential pair on the same layer and has the same number of vias. The effective length of the differential pair is the average of the length of each individual trace.

2.3.7.2 CLK/CLK#

Differential/Pair Routing Rules

CLKs are treated the same as the CAD/CAD# pairs.

CLK-to-CAD Routing Rules

The length of the CLK signal must be matched to the median of the clock group. This minimizes the combined package skew effect on TCADVRS/TCADVRH, since at most it can be the sum of the CLK-to-CAD mismatch on each package, while allowing each package to use group-trace-mismatch two times the CLK-to-CAD mismatch for the group. See the sections on TPKGskew and TPKGskewcad in the *HyperTransport™ Technology Electrical Specification*.

2.3.8 Organic Routing Rules for Signal Pairs

2.3.8.1 Route Areas and Physical Design Rules

Organic package routing tends to utilize one signal layer with three distinct areas, as shown in Figure 7.

Note: *The following design assumes minimum manufacturable design rules of 30-micron-wide traces (*w*) and 30 μm-wide minimum spaces (*s*). Designing to these minimum dimensions would result in the minimum intra-pair pitch of 60μm. This, however, would result in low trace differential impedance. The stated intra-pair pitches in the following cases maintain proper differential trace impedance while the stated inter-pair pitches reduce pair-to-pair crosstalk, all while maintaining manufacturable dimensions. These pitches represent the best trade-off between space constraints, impedance control, and crosstalk reduction.*

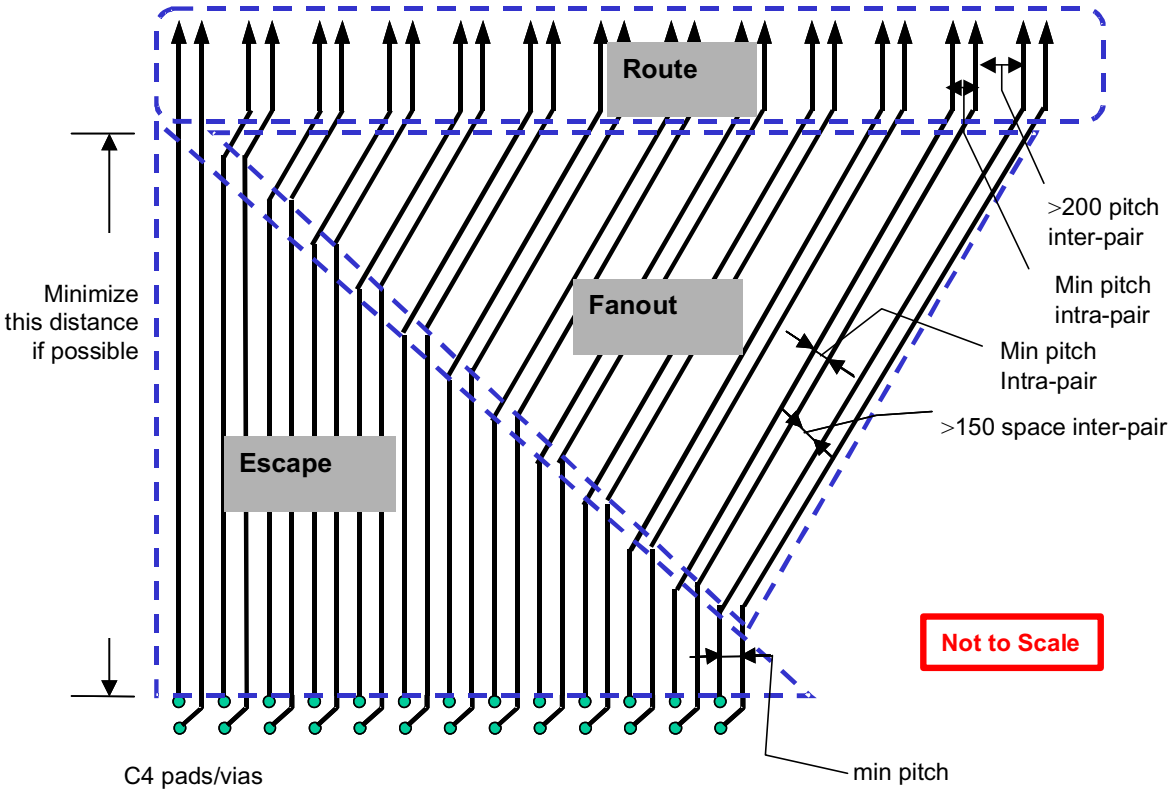


Figure 7. Organic Route Areas and Physical Design Rules

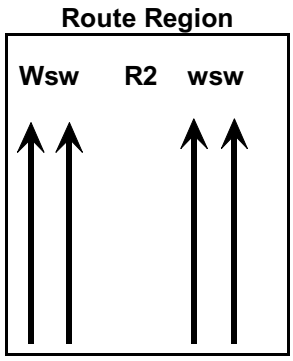


Figure 8. Organic Route Region Detail

For Micro-strip constructions (1-2-1 build-up substrates) with w = 35 µm and s = 65 µm, the single-ended impedance can be from a low of ~51 Ω to a high of 65 Ω. With R2 = 165 µm, the inter-pair pitch is 200 µm, as compared to the 100 µm intra-pair pitch.

For Stripline constructions (2-2-2 build-up substrates) with w=30 µm and s=50 µm, the single-ended impedance is ~ 44 Ω. With R2 = 170 µm, the inter-pair pitch is 200 µm, as compared to the 80 µm intra-pair pitch.

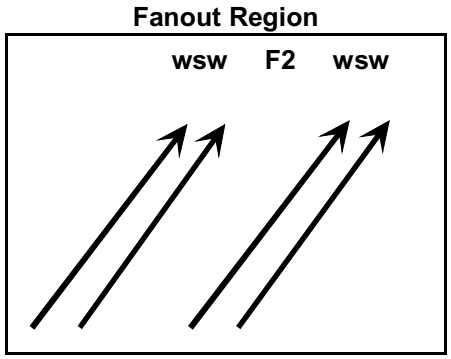


Figure 9. Organic Fanout Region Detail

For Micro-strip constructions (1-2-1 build-up substrates) with w = 35 µm and s = 65 µm, the single-ended impedance can be from a low of ~51 Ω to a high of 65 Ω. With R2 = 150 micron, the inter-pair pitch is 185 µm, as compared to the 100 µm intra-pair pitch.

For Stripline constructions (2-2-2 build-up substrates) with w=30 µm and s=50 µm, the single-ended impedance is ~35 Ω to 48 Ω. With R2 = 150 µm, the inter-pair pitch is 180 µm, as compared to the 80 µm intra-pair pitch.

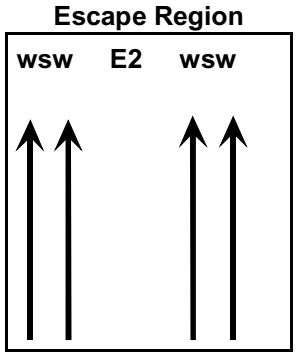


Figure 10. Organic Escape Region Detail

For Micro-strip constructions with E2 = (P – n(2w + s)) / n, where n = number of traces that route between bumps, P = flip-chip bump pitch > 200 µm, w = 35 µm and s = 35 µm (minimum), so the differential-pair-to-differential-pair spacing is the maximum allowed by the flip-chip bump pitch escape.

For Stripline constructions with E2 = (P – n(2w + s)) / n, where n = number of traces that route between bumps, P = flip-chip bump pitch > 200 µm, w = 30 µm and s = 30 µm (minimum), so the differential-pair-to-differential-pair spacing is the maximum allowed by the flip-chip bump pitch escape.

2.3.8.2 Organic Package Route Skew Control

Package skew is controlled by both minimization of electrical uncertainties and matching of the electrical length of the traces. The maximum data rate (>800 MT/s), assuming pairs are routed side by side at minimum spacing and using a signal propagation rate of 6.7 ps/mm for stripline organic packages, yields the following skew-control considerations:

- Within the differential pair, trace electrical lengths can have a maximum difference of 10 ps = 1492 µm. However, for improved signal quality, length difference should be smaller. Note that this length difference does not include the pin pitch offset caused by pins in different rows (see Section 2.3.6.3).
- Within a clock group, electrical length difference from any CAD signal (defined as the average of the two trace lengths not including the pitch offset) to the associated CLK signal can be a maximum of 10 ps = 1492 µm.
  - If CLK signal length can be made equal to the median of longest and shortest CAD signals lengths, then the total length difference within a clock group can be 20 ps = 2984 µm.
- Absolute mismatch allowed between all signals of all received clock groups is 250 ps = 37.3 mm. Absolute mismatch between all signals of all transmitted clock groups is also 250 ps = 37.3 mm.

2.3.8.3 Example Calculations

Table 13 shows some example trace lengths and highlights the package skew associated with each. In this example, either CAD[2]_H/L need to be shortened, or CLK_H/L and CAD[1]_H/L would need to be lengthened.

Table 13. Example OBGA Route Rule Calculations

Signal	Route Length (µm)	Ldiff (µm)	Time of Flight (ps)	Skew (ps) in pair	Skew (ps) to CLK
CAD[0]_H	9987	72	66.9	0.5	-1.45
CAD[0]_L	9915		66.4		
CAD[1]_H	8755	44	58.7	0.3	-9.25
CAD[1]_L	8799		59.0		
CAD[2]_H	11650	365	78.1	2.4	11.2
CAD[2]_L	12015		80.5		
CLK_H	10122	89	67.8	0.6	
CLK_L	10211		68.4		

2.3.8.4 Naturally Compensating Package Route Example

In the preceding example, the example route lengths for each differential pair could represent either the actual trace lengths or the actual trace lengths minus the natural package pitch offset. For packages implementing the naturally compensating ballout, the natural package pitch offset should be ignored to calculate both the differential skew and the signal length.

Figure 11 illustrates that for pairs with perpendicularly oriented package balls/pins, the package pitch offset is ignored. This is possible since this mismatch is negated by the equal but opposite mismatch to that of the system board traces.

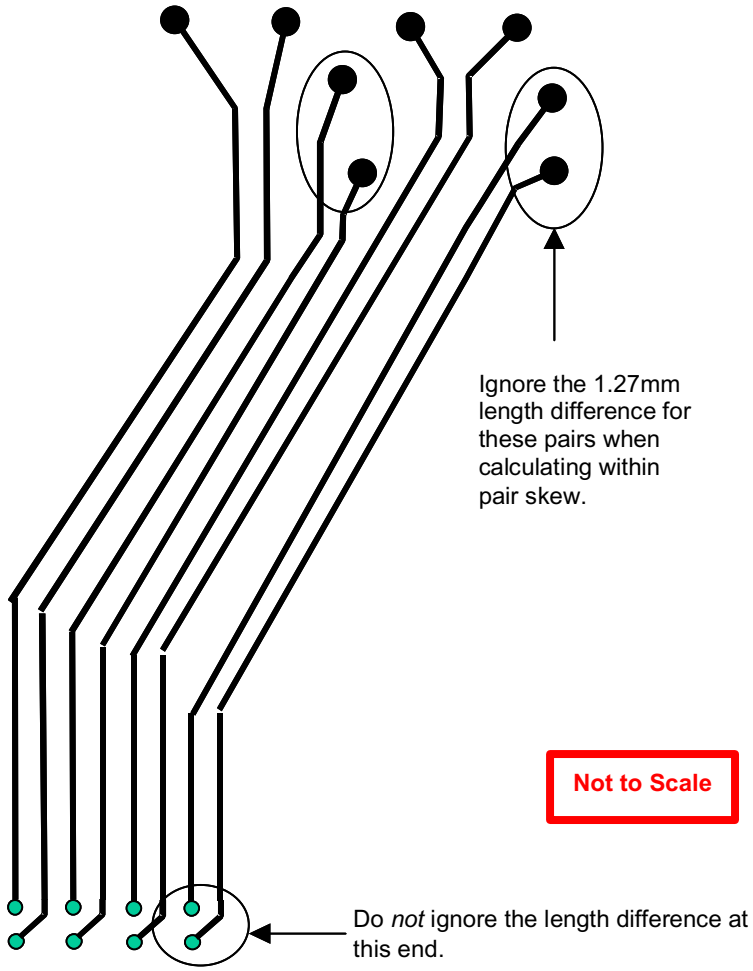


Figure 11. Organic Route MismatchesCeramic Routing Rules for Signal Pairs

Ceramic package routing tends to utilize multiple signal layers with three distinct areas, as shown in Figure 7.

Note: *The following design assumes design rules of 60 µm wide traces (*w*).*

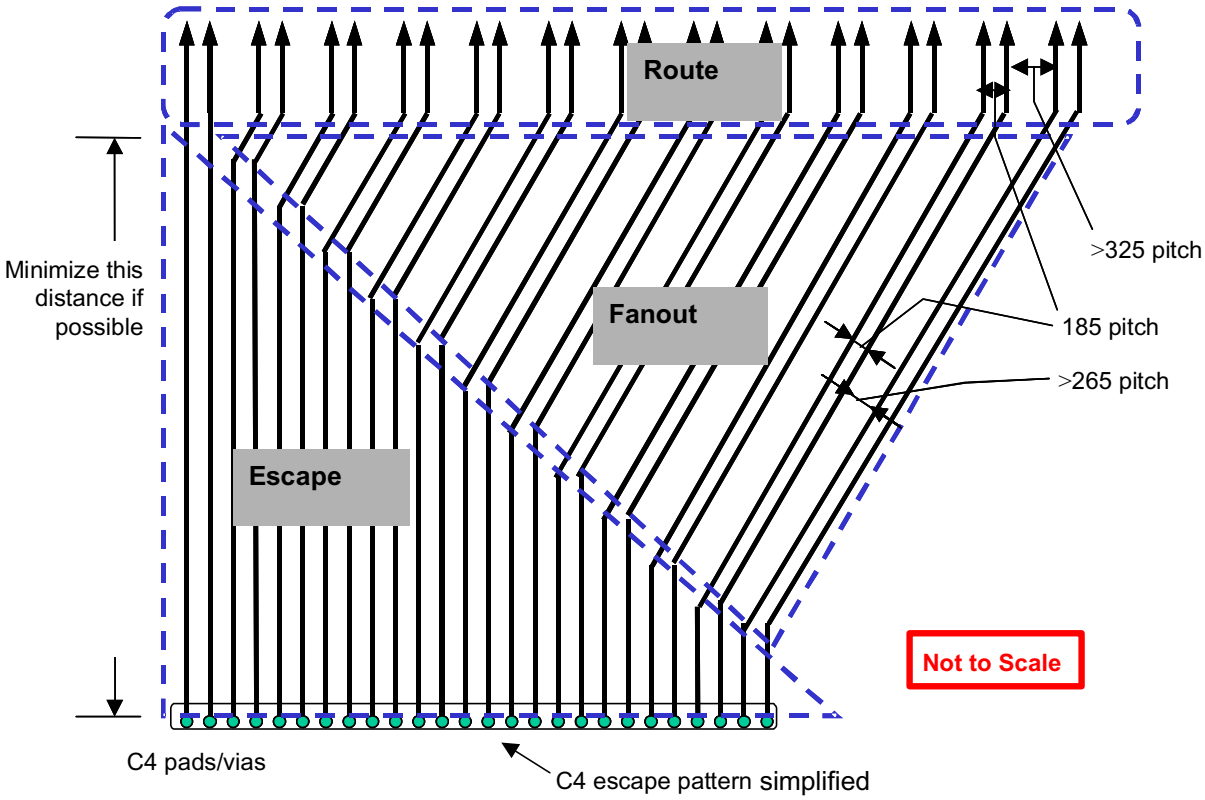


Figure 12. Ceramic Route Areas and Physical Design Rules

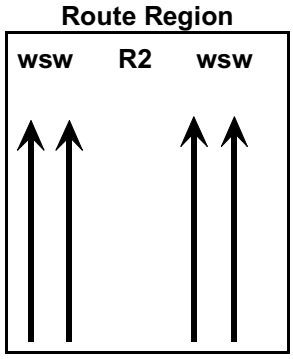


Figure 13. Ceramic Route Region Detail

With w = 60 µm and s = 125 µm, the single-ended impedance is ~44 Ω. With R2 = 265 µm, the inter-pair pitch is 325 µm, as compared to the 185 µm intra-pair pitch.

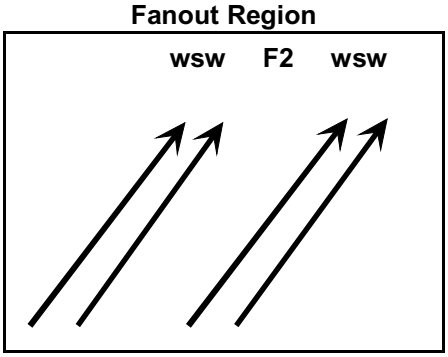


Figure 14. Ceramic Fanout Region Detail

With w = 60 µm and s = 125 µm, the differential impedance is ~44 Ω. With F2 = 225 µm, the inter-pair pitch is 285 µm, as compared to the 185 µm intra-pair pitch.

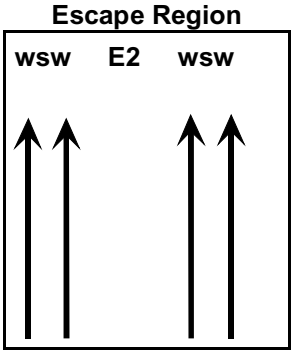


Figure 15. Ceramic Escape Region Detail

With E2 = (P – n(2w + s)) / n, where n = number of traces that route between bumps, P = flip-chip bump pitch > 250 µm, w = 60 µm and s = 90 µm, so that the differential pair to differential pair spacing is the maximum allowed by the flip-chip bump pitch escape.

2.3.9.1 Ceramic Package Route Skew Control

Package skew is controlled by both minimization of electrical uncertainties and matching of the electrical length of the traces. The maximum data rate (>800 MT/s), assuming pairs are routed side by side at minimum spacing and using a signal propagation rate of 10.6 ps/mm for ceramic packages, yields the following skew control considerations.

- Within the differential pair, electrical lengths can be a maximum of 10 ps = 943 µm. However, for improved signal quality, length difference should be smaller. This length difference does not include the pin pitch offset caused by pins in different rows (see Section 2.3.6.3).
- Within a clock group, electrical length difference from any CAD signal (defined as the average of the two trace lengths not including the pitch offset) to the associated CLK signal can be a maximum of 10 ps = 943 µm.
  - If CLK signal length can be made equal to the median of longest and shortest CAD signals lengths, then the total length difference within a clock group can be 20 ps = 1886 µm.

- Absolute mismatch allowed between all signals of all received clock groups is 250 ps = 23.6 mm. Absolute mismatch between all signals of all transmitted clock groups is also 250 ps = 23.6 mm.

2.3.9.2 Example Calculations

Table 14 shows some example trace lengths and highlights the package skew associated with each. In this example, all differential pairs are within 10 ps, and all signals are within 10 ps to the clock.

Table 14. Example Ceramic Package Route Rule Calculations

Signal	Route Length (µm)	Ldiff (µm)	Time of Flight (ps)	Skew in pair (ps)	Skew to CLK (ps)
CAD[0]_H	9588	50	101.6	0.5	-6.65
CAD[0]_L	9538		101.1		
CAD[1]_H	9355	22	99.2	0.2	-8.7
CAD[1]_L	9377		99.4		
CAD[2]_H	11000	250	116.6	2.7	9.95
CAD[2]_L	11250		119.3		
CLK_H	10166	45	107.8	0.5	
CLK_L	10211		108.2		

2.3.9.3 Naturally Compensating Package Route Example

As with the organic example, the route lengths for each differential pair could represent either the actual trace lengths or the actual trace lengths minus the natural package pitch offset. For packages implementing the naturally compensating ballout, the natural package pitch offset should be ignored to calculate both the differential skew and the signal length.

Figure 16 illustrates that for pairs with perpendicularly oriented package balls/pins, the package pitch offset is ignored. This is possible since this mismatch is negated by the equal but opposite mismatch that of the system board traces.

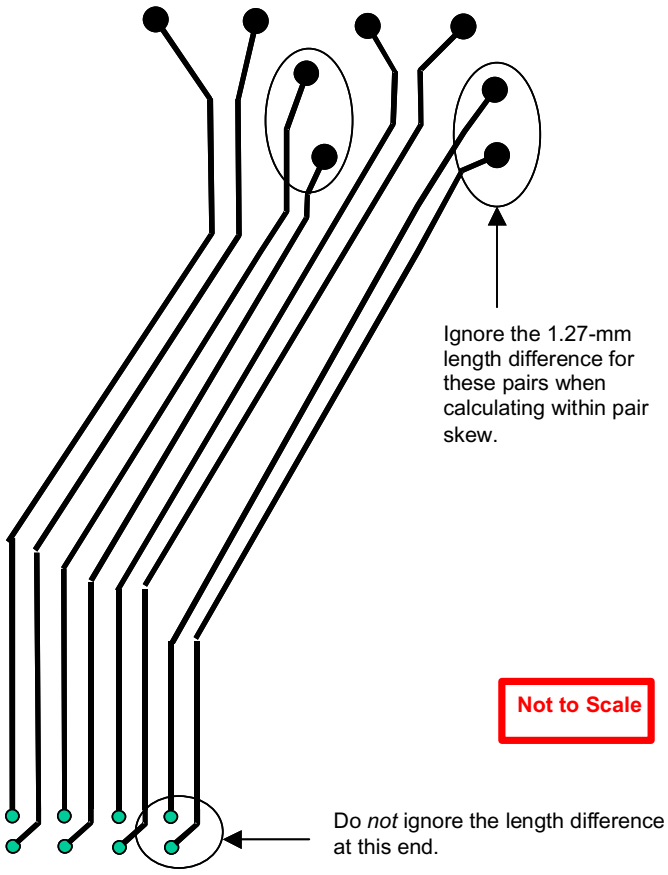


Figure 16. Ceramic Route Mismatches

2.3.10 Package Signal Crosstalk Control

In addition to simple signal trace mismatch, electrical interactions such as crosstalk and signal return path mismatch contribute to timing uncertainty of signals on the package substrate.

- To control crosstalk between separate differential pairs, maximize the spacing between neighboring traces in adjacent pairs.
  - This pitch should be no less than the spacing between traces within a pair, and preferably 1.2x or greater the intra-pair spacing, as shown in the preceding physical design rules.
- To ensure that signal propagation on the trace is deterministic and that signal quality is maintained across the trace, the path of the return current must be as similar to the wave front as possible.
  - Traces should not be routed over large holes or splits in plane layers adjacent to the trace layer in the package stackup. Such routing diverts plane return current under adjacent traces and increases crosstalk.

Some organic packages present a special case. For manufacturing reasons, their planes require regularly spaced voids. In this case, special care should be taken to control the placement of the voids relative to differential pairs. If possible, reshape and/or redistribute the voids in the trace route region so that traces do

not overlay holes, or overlay only the edges of holes. If holes must be crossed over with traces, attempt to ensure that traces within a differential pair cross over the same holes, and traces in separate differential pairs do not cross over the same holes (see Figure 17).

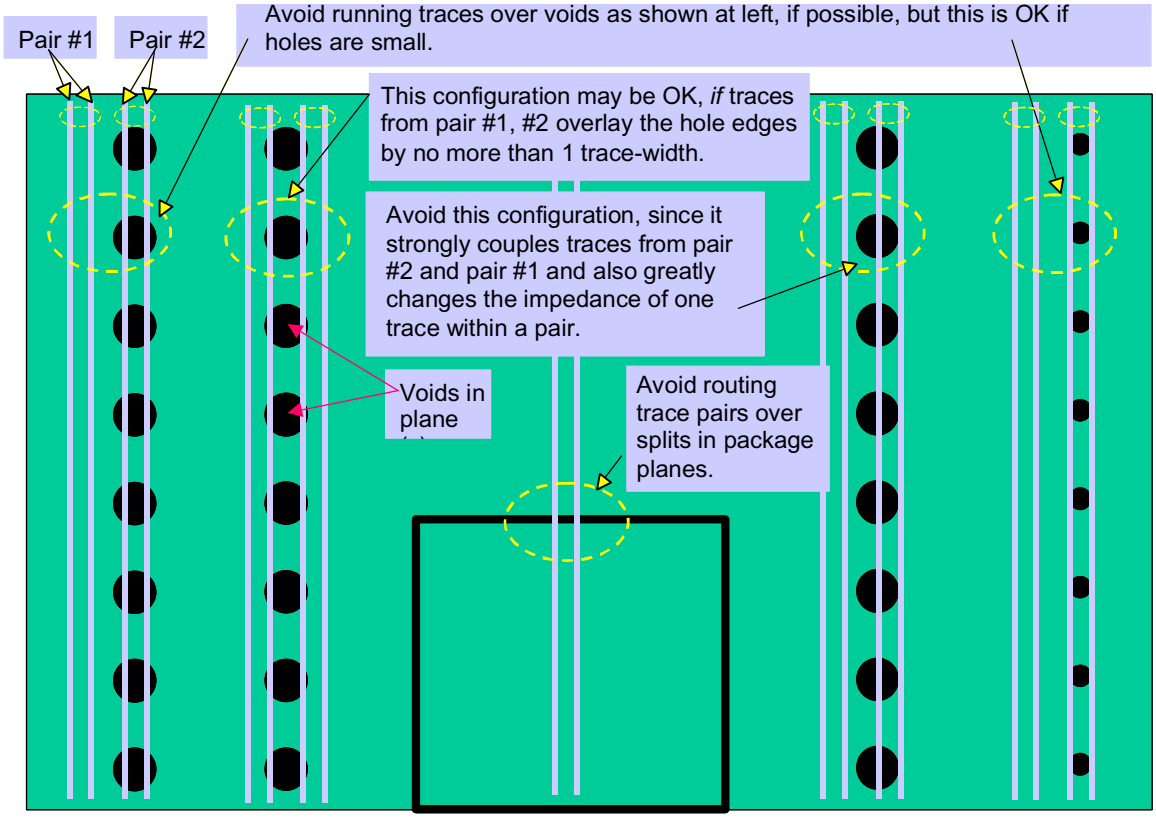


Figure 17. Crosstalk Control—Flip-Chip OBGA Example

2.3.11 Crosstalk Control for Wirebond Packages

For signal-integrity reasons, it is strongly preferred that flip-chip packages be used for all HyperTransport device packages. However, if a wirebond OBGA is used (only for HyperTransport data rates of 400 MT/s), some rules must be followed for signal wirebonds:

- Wirebonds for all signals must be as short as possible (< 6 mm).
- Pads and wirebonds for the two lines comprising a differential pair must be immediately adjacent to each other on the die and the package, and bonds must be essentially the same length (ignoring the die-pad stagger).
- One VSS or VDD wirebond should be inserted between adjacent differential pair bonds if possible (preferably alternating VSS/VDD, as shown in Figure 18).
- Clock differential pairs should be made especially short if possible, and it is desirable to include one VSS and one VDD bond adjacent to each side of a clock pair.
- VLDT wirebonds should be made as short as practical.

- VSS wirebonds may be used as shields between the HyperTransport pairs and any adjacent non-HyperTransport signals to reduce crosstalk in the wirebonds. These shield VSS wirebonds can be made as long as practical.

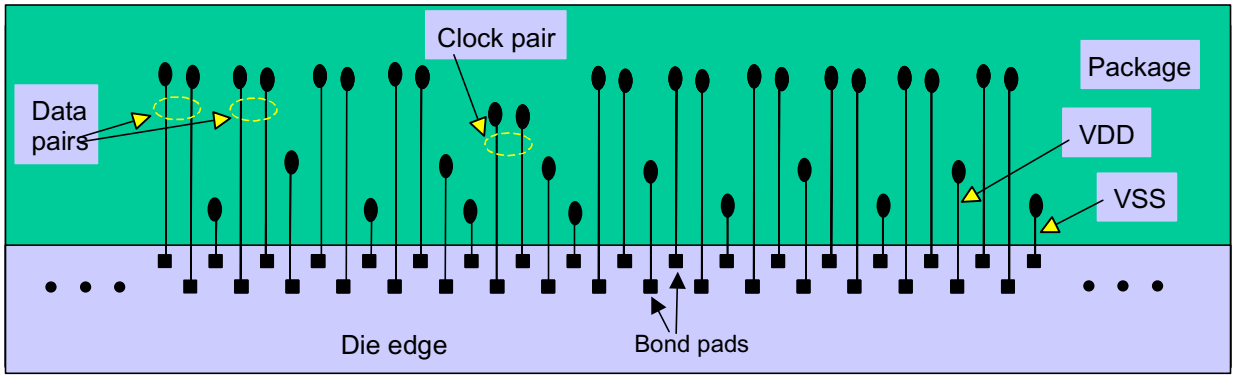


Figure 18. Crosstalk for Wirebond Packages

2.4 System Board Design Guidelines

2.4.1 Conceptual Electrical Description

The HyperTransport electrical interface is a low-swing differential signal from an impedance-controlled driver (R_{ON}) driving a differential receiver with on-die differential termination (R_{TT}). A conceptual circuit is shown in Figure 19. R_{ON} acts as source termination and R_{TT} acts as the load termination with the following relationships:

- $R_{ON} = Z_{OD} / 2$
- $R_{TT} = Z_{OD}$

With these relationships met, the physical board stackup and trace/space will result in single-ended characteristic impedance. In this design guide, the recommended trace and space widths and the recommended dielectric thickness and properties achieve a single-ended characteristic impedance of 60 Ω. The tolerance on this single-ended trace impedance is relatively large (±17%) because the priority should be on matching the differential impedance of the trace pair to both the 2 * R_{ON} and to R_{TT}.

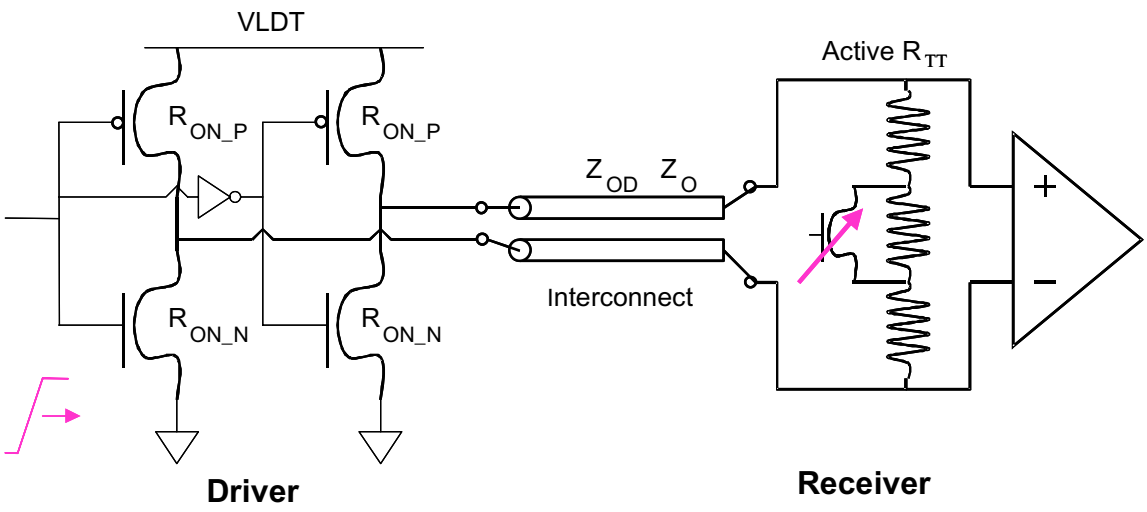


Figure 19. HyperTransport Technology Conceptual Circuit

2.4.2 System Board Stackup Guidelines

HyperTransport links can be implemented on system boards using as few as one signal layer to as many signal layers as there are clock groups. Four-layer (two signal, two plane) to eight-layer (two signal, two plane) are expected to be the system board layer counts of choice. The system board stackups illustrated in Figures 20, 21, and 22 are recommended to meet the required trace impedances.

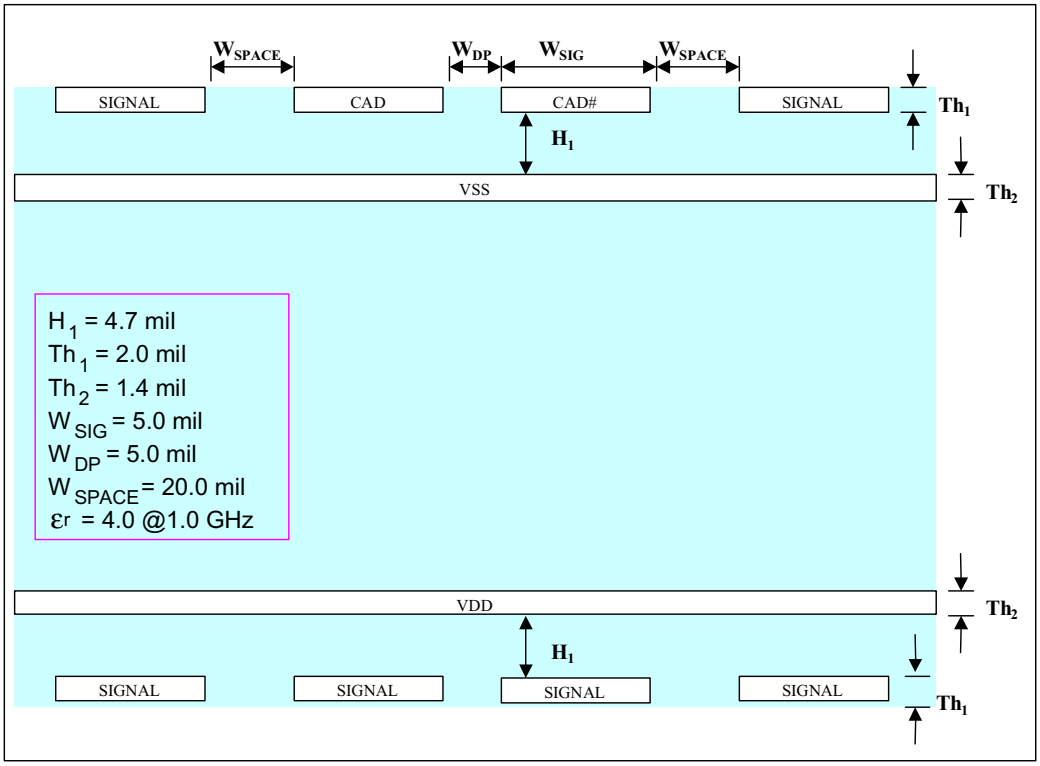


Figure 20. Four-Layer System Board Stackup

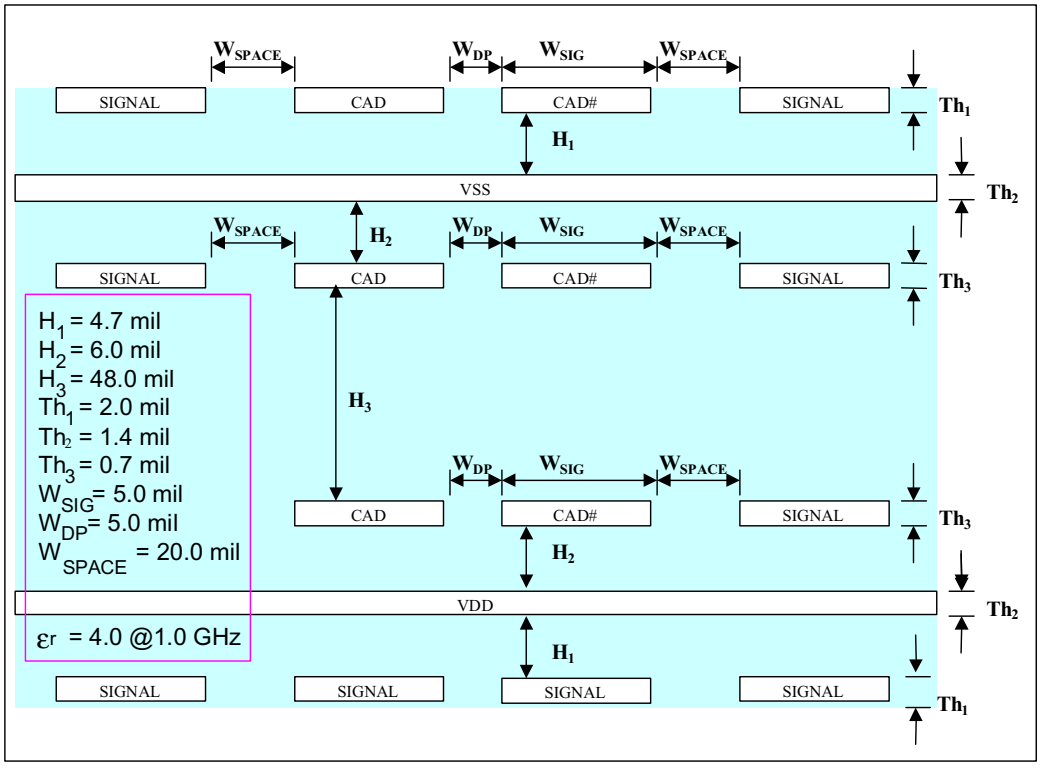


Figure 21. Six-Layer System Board Stackup

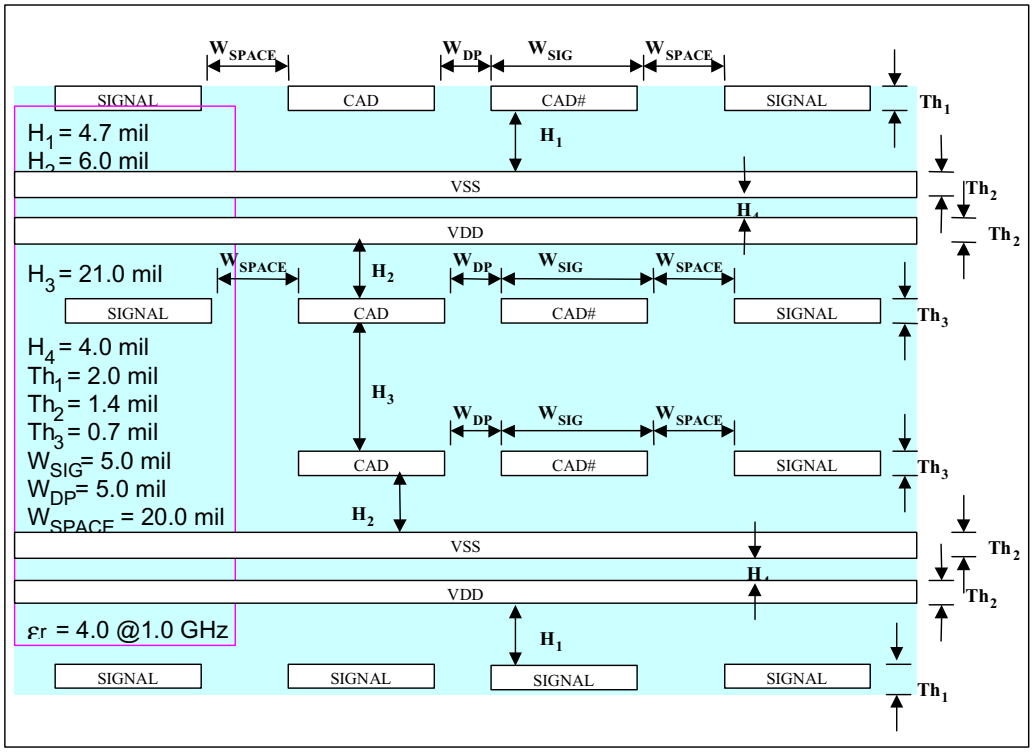


Figure 22. Eight-Layer System Board Stackup

2.4.3 System Board Trace Electrical Specification

The materials and technologies must be selected to obtain electrical characteristics of system board traces as follows:

- Z_O = 60 Ω ±17% (50–70 Ω) (covers manufacturing variances in micro-strip traces)
- Z_{OD} = 100 ±10% (90–110 Ω) (covers manufacturing variances in micro-strip traces)
- Maximum R_{DC} = 0.29 Ω/in
- Maximum R_{AC} = 1.50 Ω/in @1 GHz
- Maximum G_{AC} = 0.32 S/in @1 GHz
- T_{PD} = 150–170 ps/in
- T_{PD_ODD} = 135–155 ps/in

2.4.4 System Board Trace Routing Guidelines

System boards containing HyperTransport devices must consider both timing uncertainty and signal integrity of the signals. General rules for system board design are included in Table 15. These rules assume propagation rates of 150 ps/in for micro-strip constructions and 180 ps/in for stripline constructions.

Table 15. Overview of System Board Design Rules

Description		Definition/Parameter[1]	Rules[2]		
1a	_H to _L trace length matching (differential skew) using trace-by-trace compensation	Defines the absolute length difference allowed between _H and _L signal traces. Parameter=DiffPCBskew 400–800 MT/s = 20 ps >800 MT/s = 5 ps	**Link Speed**	**Micro-strip[3]**	**Stripline[4]**
			400 MT/s	133	111
			600 MT/s	133	111
			800 MT/s	133	111
			1000 MT/s	33	28
			1200 MT/s	33	28
			1600 MT/s	33	28
1b	_H to _L trace length matching (differential skew) using zero mismatch boundaries	Defines the absolute length difference allowed between _H and _L signal traces. Parameter=DiffPCBskew 400–800 MT/s = 20 ps >800 MT/s = 5 ps	400 MT/s	133	111
			600 MT/s	133	111
			800 MT/s	133	111
			1000 MT/s	33	28
			1200 MT/s	33	28
			1600 MT/s	33	28
1c	_H to _L trace length matching (differential skew) using	Defines the absolute length difference allowed between _H and _L signal traces. For perpendicularly oriented	400 MT/s Parallel Perpendicular	133 pitch +/- 133	111 pitch +/- 111

Description		Definition/Parameter[1]	Rules[2]		
	skew) using naturally compensating matching[5]	perpendicularly oriented package pins, the target trace mismatch is equal to the pin pitch with positive tolerance to limit the maximum trace mismatch or negative tolerance to limit the minimum trace mismatch. Parameter = DiffPCBskew 400–800 MT/s = 20 ps >800 MT/s = 5 ps	600 MT/s Parallel Perpendicular	133 pitch +/- 133	111 pitch +/- 111
			800 MT/s Parallel Perpendicular	133 pitch +/- 133	111 pitch +/- 111
			1000 MT/s Parallel Perpendicular	33 pitch +/- 33	28 pitch +/- 28
			1200 MT/s Parallel Perpendicular	33 pitch +/- 33	28 pitch +/- 28
			1600 MT/s Parallel Perpendicular	33 pitch +/- 33	28 pitch +/- 28
2	CAD/CTL/CLK trace lengths	Defines the minimum and maximum overall trace lengths.	**Link Speed**	**Min/Max.**	
			400–800 MT/s	1 in/24 in	
			> 800 MT/s	1 in/12 in	
3	CLK to CAD/CTL trace length matching (CLK centering)	Defines the length difference allowed between the longest or shortest average of _H and _L for any CAD/CTL signal within a clock group and the average length of _H and _L for the associated CLK. Parameter = TPCBskew	**Link Speed**	**Micro-strip**	**Stripline**
			400 MT/s	333	276
			600 MT/s	333	276
			800 MT/s	200	167
			1000 MT/s	133	111
			1200 MT/s	100	84
			1600 MT/s	67	34
4	CAD/CTL to CAD/CTL trace length matching (group skew)	Defines the length difference allowed between the longest and shortest average of _H and _L for all CAD/CTL signals within a clock group. Parameter = TPCBskewcad[6]	**Link Speed**	**Micro-strip**	**Stripline**
			400 MT/s	667	555
			600 MT/s	667	555
			800 MT/s	400	333
			1000 MT/s	266	222
			1200 MT/s	200	167
			1600 MT/s	133	111
5	CAD/CTL group to CAD/CTL group[7]	Defines the length difference allowed between the longest or shortest average of _H and _L of one CAD/CTL OUT	**Link Speed**	**Micro-strip**	**Stripline**
			400 MT/s	3333	2778

Description		Definition/Parameter[1]	Rules[2]		
	group[7]	_L of one CAD/CTLOUT group to the shortest or longest average of _H and _L of another CAD/CTLOUT group. There is no need to maintain this rule between a receive group and a transmit group. Parameter = Rclk2Rclkskew (Divided equally between package and system board) = 500 ps	600 MT/s	3333	2778
			800 MT/s	3333	2778
			1000 MT/s	3333	2778
			1200 MT/s	3333	2778
			1600 MT/s	3333	2778
6	CAD/CTL/CLK trace width (*tr*) and spacing (*sp*)	Recommended system board trace width and space. Parameter = Z_O, Z_{OD}	**Link Speed**	**Micro-strip sp/tr/sp/tr/sp**	**Stripline sp/tr/sp/tr/sp**
			400 MT/s	20/5/5/5/20	20/5/5/5/20
			600 MT/s	20/5/5/5/20	20/5/5/5/20
			800 MT/s	20/5/5/5/20	20/5/5/5/20
			1000 MT/s	20/5/5/5/20	20/5/5/5/20
			1200 MT/s	20/5/5/5/20	20/5/5/5/20
			1600 MT/s	20/5/5/5/20	20/5/5/5/20
7	CAD/CTL/CLK impedance control and stackup	Recommended dielectric thickness from signal layer to plane layer	**Micro-strip**	**Stripline**	
			4.7	6.0	

Notes:

1. *Parameter references are to the detailed transfer timing budget found in appendices K and L of the* HyperTransport™ I/O Link Specification*, Rev. 1.03.*
2. *Units are in mils.*
3. *Propagation rate used for micro-strip constructions is 150 ps/in.*
4. *Propagation rate used for stripline constructions is 180 ps/in.*
5. *Relative lengths of _H and _L between the package and the motherboard need to reverse to achieve the length compensation. For example, if _H trace is shorter than _L trace on the package, then _H trace must be longer on the motherboard than _L trace.*
6. *TPCBskewcad is merely 2 times the TPCBskew allowed, and therefore if these rules are met, TPCBskewcad is met also.*
7. *CAD-group-to-CAD-group mismatches allowances are extreme not-to-exceed numbers. Good design should easily maintain mismatch significantly lower than these maximums.*

2.4.5 Trace-Length Mismatch Control

The choice of trace mismatch control method also affects the method by which the trace lengths on the system board are compared.

2.4.5.1 Trace-by-Trace Compensated Matching

When using trace-by-trace compensated matching, the system board trace length must compensate for the mismatch in the package trace lengths on a trace-by-trace basis. Effectively, the length of system board trace must be lengthened or shortened to compensate for short or long traces on the transmitter or receiver package. The following steps would result in this type of trace matching:

- Gather trace-by-trace length data for both transmitter and receiver packages.
- Identify the longest system board trace within each clock group (use Manhattan distances for approximation).
- Route the longest signal (differential pair) so the differential skew specification is met, and determine effective pad-to-pad signal length (adding transmitter and receiver package trace electrical lengths).
- Assign length rule to each remaining signal trace such that the system board trace length plus the sum of the package trace electrical lengths equals the effective pad-to-pad signal length of the longest signal within the clock group.
- Route the rest of the clock group.
- Extract resulting system board trace lengths and add the sum of the package electrical lengths to determine if skew control has been maintained.

2.4.5.2 Zero-Mismatch Boundaries

Zero-mismatch boundaries for most system-board layout design software must use transparent-component or test-point symbols on each end of the trace to identify the physical location of the zero-mismatch boundary, along with providing a measurement point from which trace lengths can be referenced. The goal of this method of trace length matching is to define two physical boundary points where the trace mismatch of both the differential pair and within the clock group is 0. The following steps would result in this type of matching:

- Gather trace-by-trace length data for both transmitter and receiver packages.
- Insert into the schematic symbols that can be recognized by the layout design software as components yet not create any distortions in the actual drawn trace. These symbols will be used to identify the physical location of the zero-mismatch boundary and to allow for trace matching measurement between segments of the trace.
- Place zero-mismatch boundary symbols physically relative to some object so that the resulting trace length between them can be equalized. At each package boundary is one possible physical location for the zero-mismatch boundary points.
- Identify the longest system board trace within each clock group (use Manhattan distances for approximation) between the zero-mismatch boundary points.
- Route the longest system board trace from the transmitter package pins to the zero-mismatch boundary points. Either adjust the location of the zero-mismatch boundary points so the electrical lengths of each trace from the pad to the zero-mismatch boundary point are equal, or route each so that they are equal.

- Route the longest system board trace from the receiver package pins to the zero-mismatch boundary points. Either adjust the location of the zero-mismatch boundary points so the electrical lengths of each trace from the pad to the zero-mismatch boundary point are equal, or route each so that they are equal.
- Route the longest system board signal between the zero-mismatch boundary points.
- Use the signal length between the zero-mismatch boundary points to assign length rules to each additional signal within the clock group.
- Use the longest signal transmitter segment length and the transmitter package trace electrical lengths to assign length rules to the remaining transmitter segments.
- Use the longest signal receiver segment length and the receiver package trace electrical lengths to assign length rules to the remaining receiver segments.
- Extract resulting system board trace lengths and add the sum of the package electrical lengths to determine if skew control has been maintained.

2.4.5.3 Naturally Compensating Matching

Use the following steps to match signals using the naturally compensating matching method:

- Determine which traces are contained in the following four classes of nets per clock group:
  - No Package Offset—This class contains traces of differential pairs that have both balls/pins oriented parallel to the package edge in the same row. Note that the recommended pinouts in this guide would not result in any traces in this class.
  - One-Package Offset Long—This class contains traces of differential pairs that are one package-pitch longer than their complement due to perpendicularly oriented package balls/pins.
  - One-Package Offset Short—This class contains traces of differential pairs that are one package-pitch shorter than their complement due to perpendicularly oriented package balls/pins.
  - Two-Package Offset Short/Long—This class would contain traces that are two package-pitches shorter or longer than their complement. Note that the recommended pinouts in this guide would not result in any traces in this class.
- Identify the longest system board trace within each clock group (use Manhattan distances for approximation) from package to package.
- Making sure to break all signals out towards the package edge, route the longest signal such that the mismatch between true and complement is within the length rule tolerance of the package pitch.
- Use the measured length of the one-package-offset-short class to assign length rules to the remaining one-package-offset-short traces and route them.
- Use the measured length of the one-package-offset-long class to assign length rules to the remaining one-package-offset-long traces and route them.
- Extract resulting system board trace lengths and add the sum of the package electrical lengths to determine if skew control has been maintained.

The case may also occur where a device with a slow 8x8-bit ballout is to connect to a device with a fast 8x8-bit ballout. In this case, the low-order nibble would route just as the case above. However, the high-order nibble will cause elongated system board routes. These longer traces will set the nominal group trace length. This length would then be adjusted by any naturally occurring package offset within differential pairs. Note also that this case only occurs for slow links, and therefore the tolerance on the matching requirements is significantly increased, making these targets much more easier to implement.

2.4.6 System Routing Rules for Individual Signal Groups

General Routing Rules

- Routing physical rules are:
  - Trace width and trace spacing within differential pairs = 5 mils
  - Trace spacing between differential pairs = 20 mils
  - Same net spacing (minimum distance from a trace to itself) = 50 mils
- All signals are ground-referenced differential pairs.
- All HyperTransport signals are referenced to VSS, VDD, or VLDT.
- All termination is provided on-die. No termination is required on the motherboard. R_{TT} termination and driver R_{ON} are configurable through a combination of resistor values and register settings.

Differential Routing Rules

- Each trace within the differential pair is routed on the same layer and has the same number of vias. Trace length within the pair is measured absolutely.

Pair Routing Rules

- CAD/CAD# and CTL/CTL# within a clock group should be treated identically. Each signal is routed as a differential pair on the same layer and has the same number of vias for link frequencies above 800 MT/s.
- For link frequencies of 800 MT/s or less, multiple layers may be used. However, trace length must be inserted on top-layer nets to approximately match the extra delay due to vias for bottom-layer nets.
  - Clock groups should never be split between traces routed on inner and outer layers or between layers with different nominal propagation speeds.
  - Decoupling between the reference plane layers is required in the vicinity of the layer transition.
- The effective length of the differential pair is the average of the lengths of the traces in that pair.

2.4.7 Routing Rules for Reference Clocks

Reference clocks for HyperTransport devices have rules restricting the time variant phase error as seen by the transmitter and receiver relative to one another. However, there are no limitations on the time invariant skew resulting from these reference clocks being routed with mismatched trace lengths.

2.4.8 Routing Rules Between Clock Groups

The mismatch allowed between the CLK signals of transmitting clock groups is limited to bound the amount of reference clock time variant phase error that can be tolerated by the nominal receiver phase recover FIFO. This mismatch is limited to 500 ps or 3333 mils for micro-strip implementations or 2778 mils for stripline implementations.

2.4.9 Physical Layer Usage

2.4.9.1 16x16-Bit Two-Signal-Layer High-Speed (>800 MT/s) Breakout

The 16x16-bit two-layer high-speed breakout (shown in Figure 23) uses the top-route layer for all signals (including CADIN and CADOUT) within the transmit and receive low byte clock groups. It uses the bottom layer for all signal layers within the transmit and receive high byte clock groups. This layer usage works with system boards down to those with only two signal layers, without introducing skew inherent with signals routed on different layers or transitions between layers into the transfer timing budget.

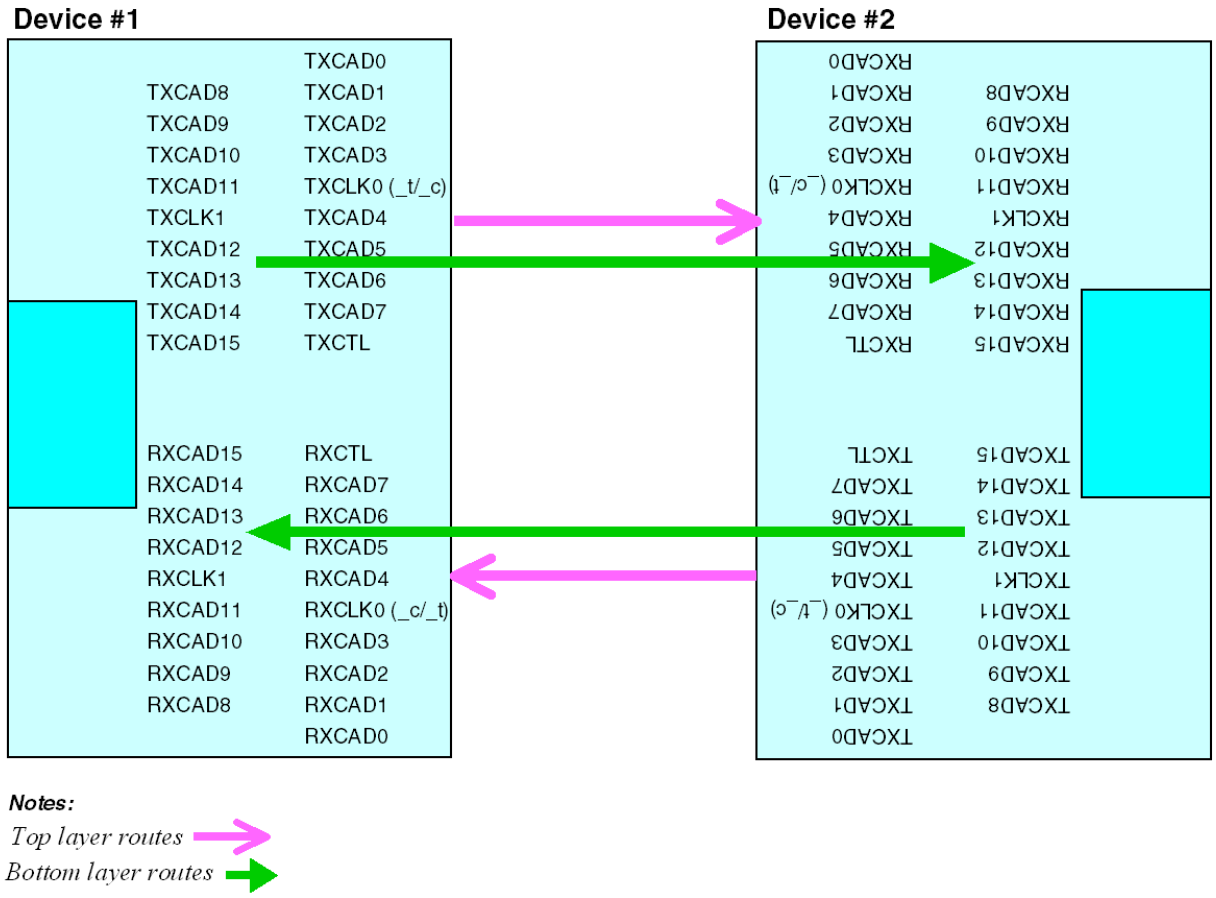


Figure 23. 16x16-Bit Two-Signal-Layer Breakout and Layer Usage

2.4.9.2 8x8-Bit One-Signal-Layer High-Speed (>800 MT/s) Breakout

The 8x8-bit one-layer high-speed breakout shown in Figure 24 uses the top-route layer for all signals (including CADIN and CADOUT). This layer usage works with system boards with only two signals layers, without introducing skew inherent with signals routed on different layers or transitions between layers into the transfer timing budget.

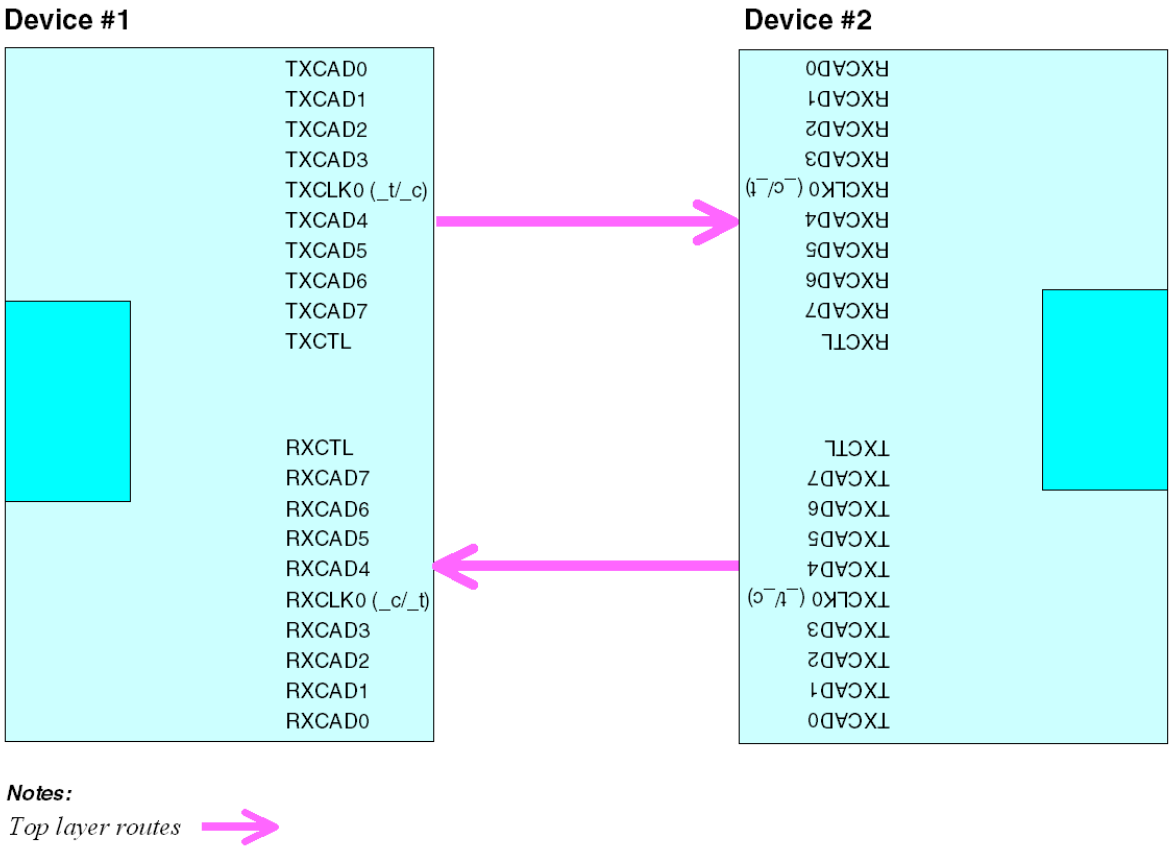


Figure 24. 8x8-Bit One-Signal-Layer Breakout and Layer Usage

2.4.9.3 8x8-Bit Two-Signal-Layer Low-Speed (≤800 MT/s) Breakout

- Use two layers for each clock/data group (split high and low nibble).
  - CTL routes with lower order nibble.

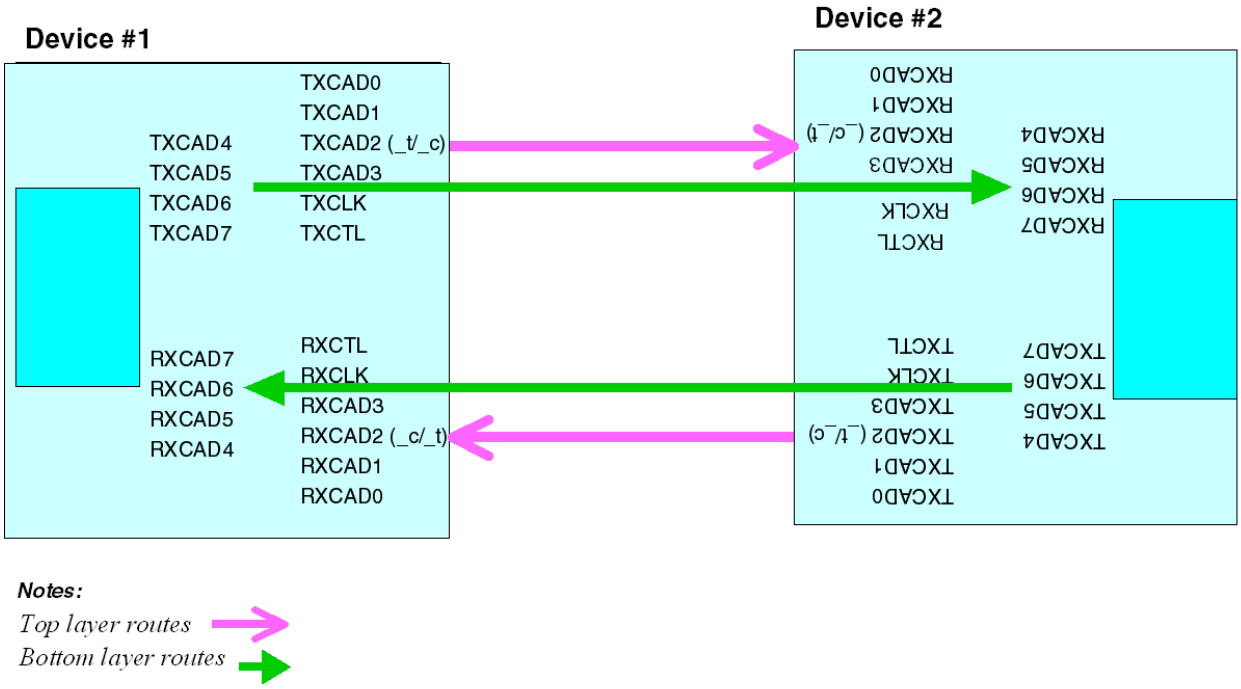


Figure 25. 8x8-Bit Two-Signal-Layer Breakout and Layer Usage

2.4.9.4 8x8-Bit Low-Speed (≤800 MT/s) to 4x4-Bit One-Signal-Layer Breakout

Devices are connected in both directions. The breakout requires the following:

- Use one layer for the entire link.

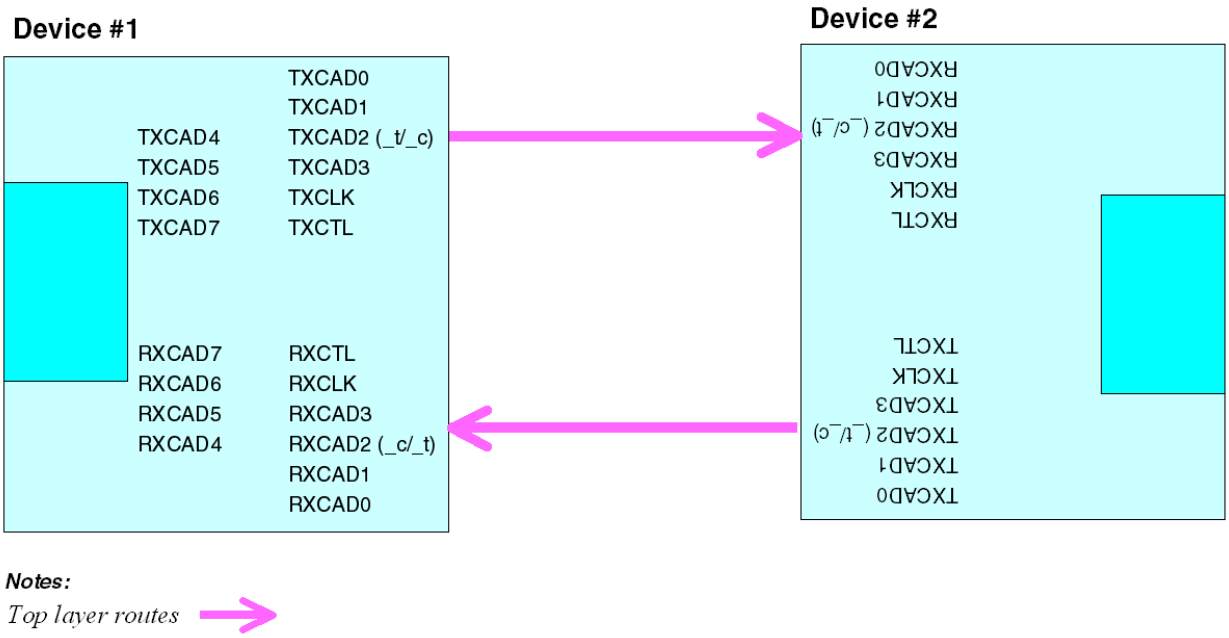


Figure 26. 8x8-Bit to 4x4-Bit One-Signal-Layer Breakout and Layer Usage

2.4.9.5 4x4-Bit One-Signal-Layer Breakout

- Use one layer for entire link.

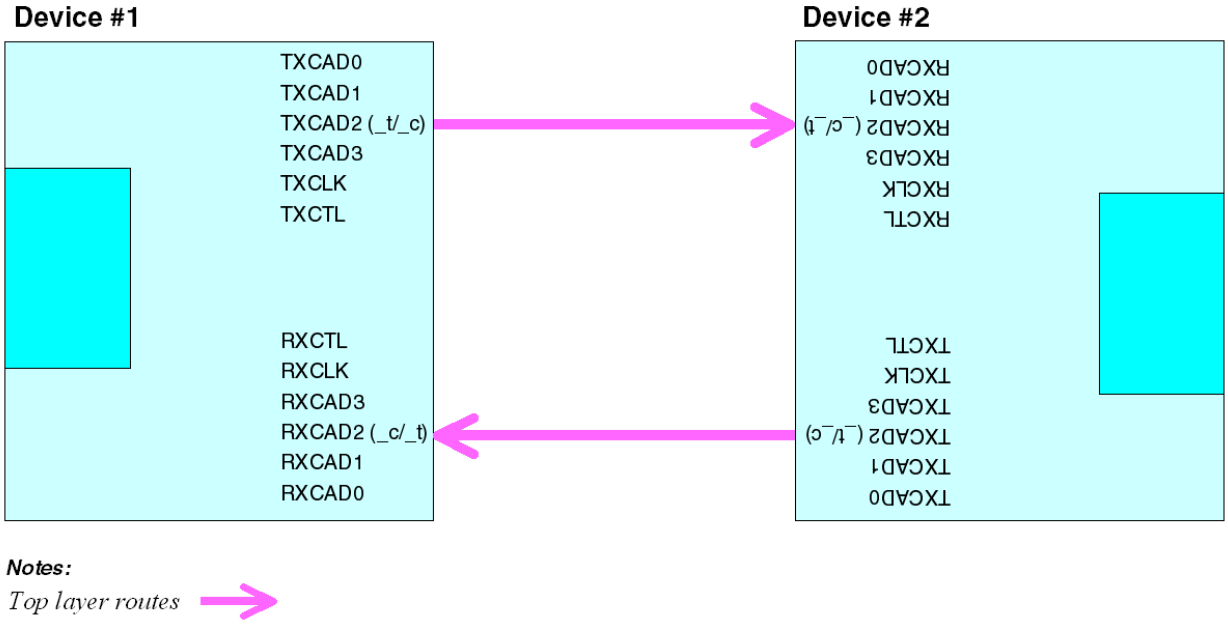


Figure 27. 4x4-Bit One-Signal-Layer Breakout and Layer Usage

2.4.9.6 16x16-Bit High-Speed to 8x8-Bit Low-Speed Two-Signal-Layer Breakout

Devices are connected in both directions. The breakout requires the following:

- CADOUT[7:4] to transition layers (top to bottom)
- CADIN[7:4] to transition layers (bottom to top)
- CADOUT[3:0], CTLOUT, CADIN[3:0], and CTLIN route on top layer

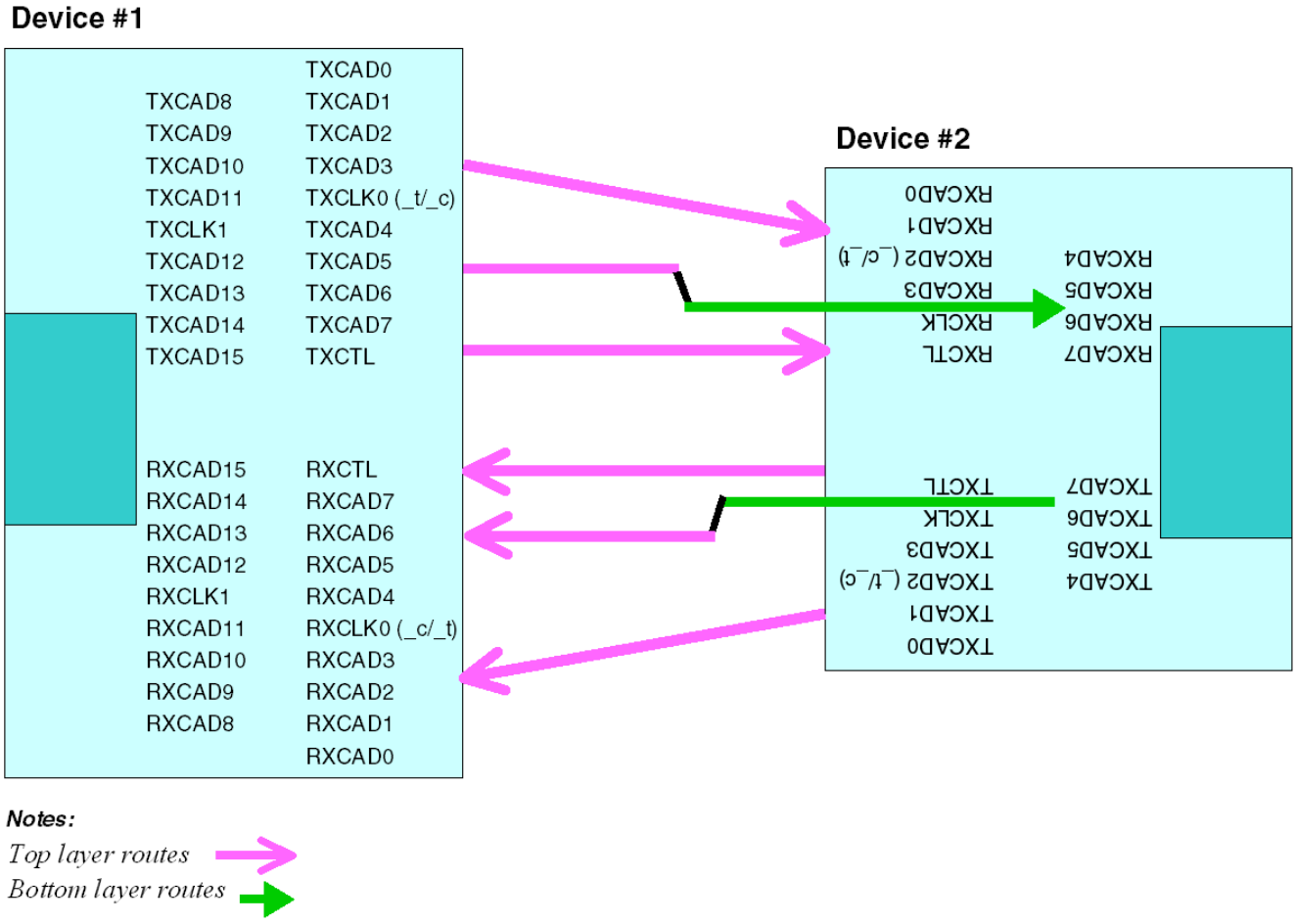


Figure 28. 16x16-Bit to 8x8-Bit Two-Signal-Layer Breakout and Layer Usage

2.4.10 Trace Referencing

HyperTransport is a ground-referenced differential bus. Differential pairs are weakly coupled and reference the coupled plane more than they reference each other. This referenced plane is ideally VSS, but can also be VDD (some other DC voltage plane) or VLDT.

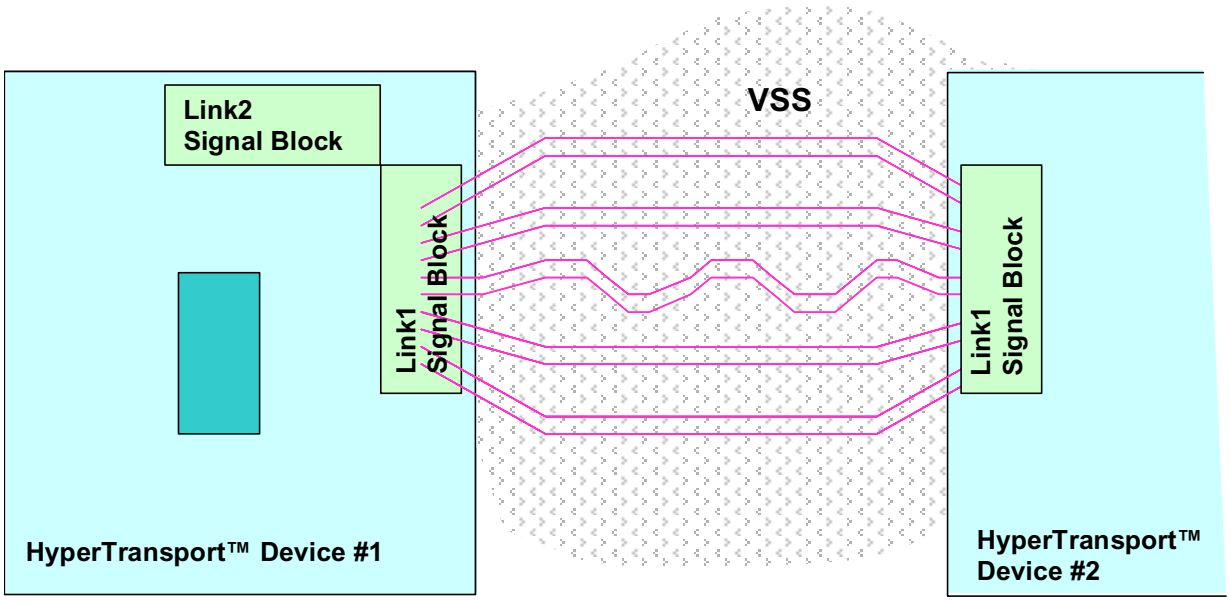


Figure 29. VSS-Referenced Layout

2.4.11 Changes in Trace Referencing

Some precautions must be taken when there is a change in the reference plane for the differential pairs due to crossing plane splits or changing signal layers (only recommended for links at 800 MT/s or slower). Following is a list of precautions:

- The plane separation should be 15 mils or less.
- If a clock/data group changes layers, place the vias on each of the traces within the individual pairs as close as possible to prevent a major differential impedance discontinuity. It is acceptable for the via antipad plane clearances to overlap in this instance. Vias between pairs should be spaced apart by a minimum of 50 mils to reduce coupling between the pairs.
  - One 0.01 µF 0603 capacitor is used to bridge the referenced planes at the layer change for every four diff-pairs. This helps minimize crosstalk in the return path signal. See Figure 30.
- If a clock/data group crosses a plane split in the referenced plane, one 0.01 µF 0603 capacitor is used to bridge the split in the referenced planes. This will help minimize the crosstalk in the return path signal. See Figure 31.

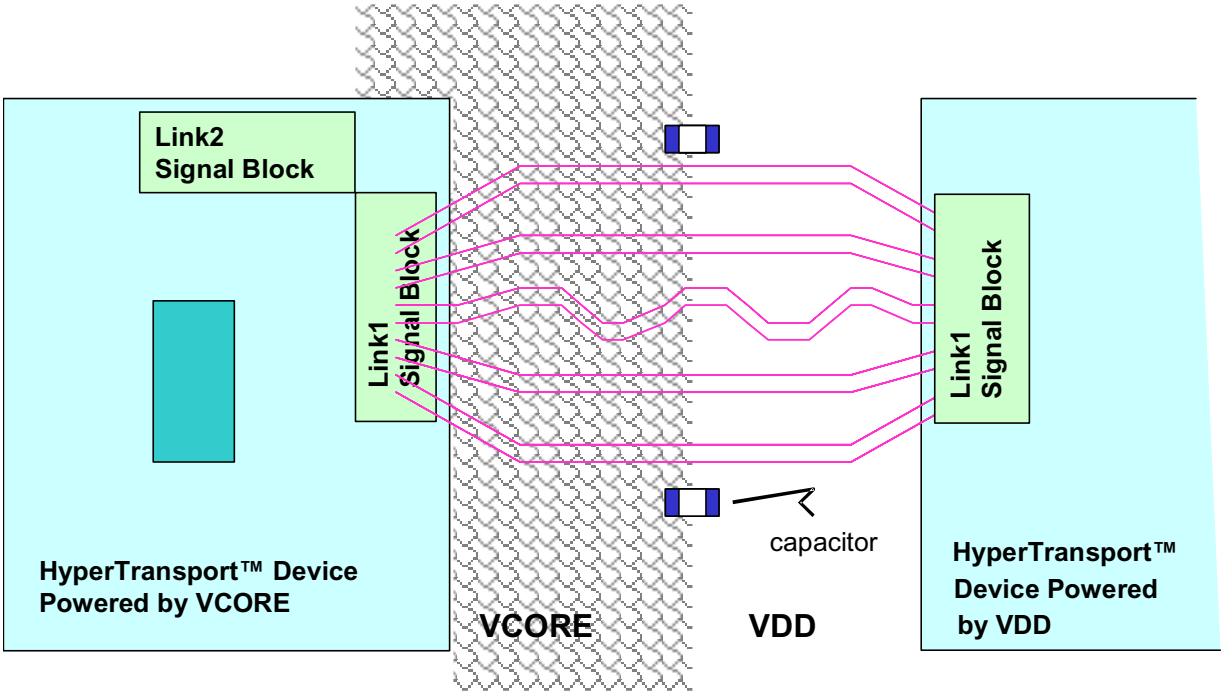


Figure 30. Return Path for Signals Changing Layers

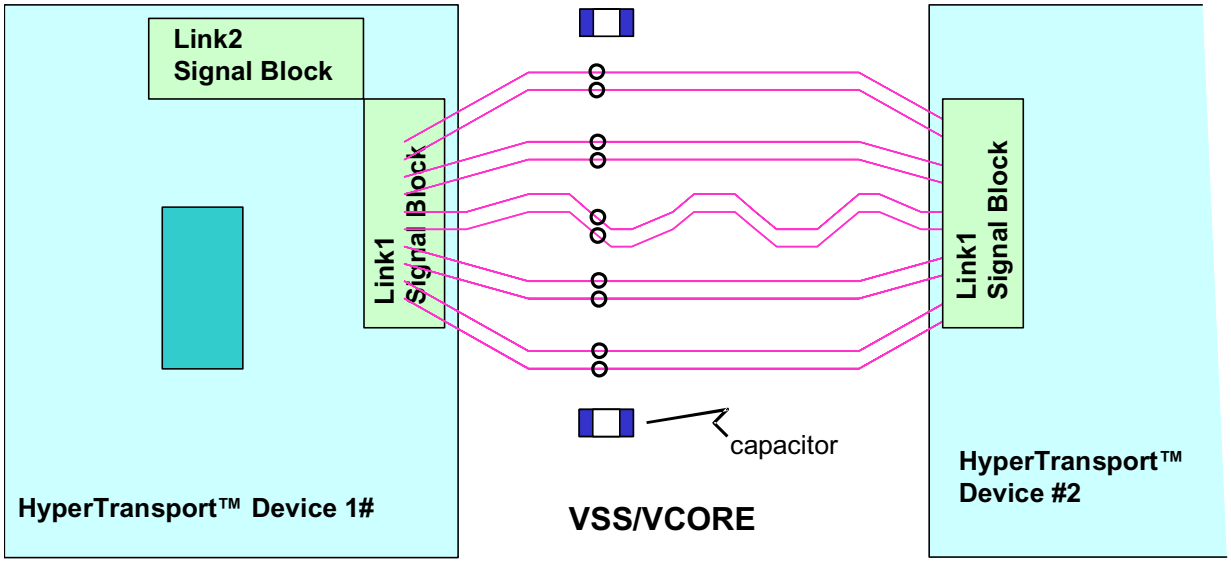


Figure 31. Return Path for Signals Crossing Plane Splits

2.4.12 Two-Signal-Layer Routing Example

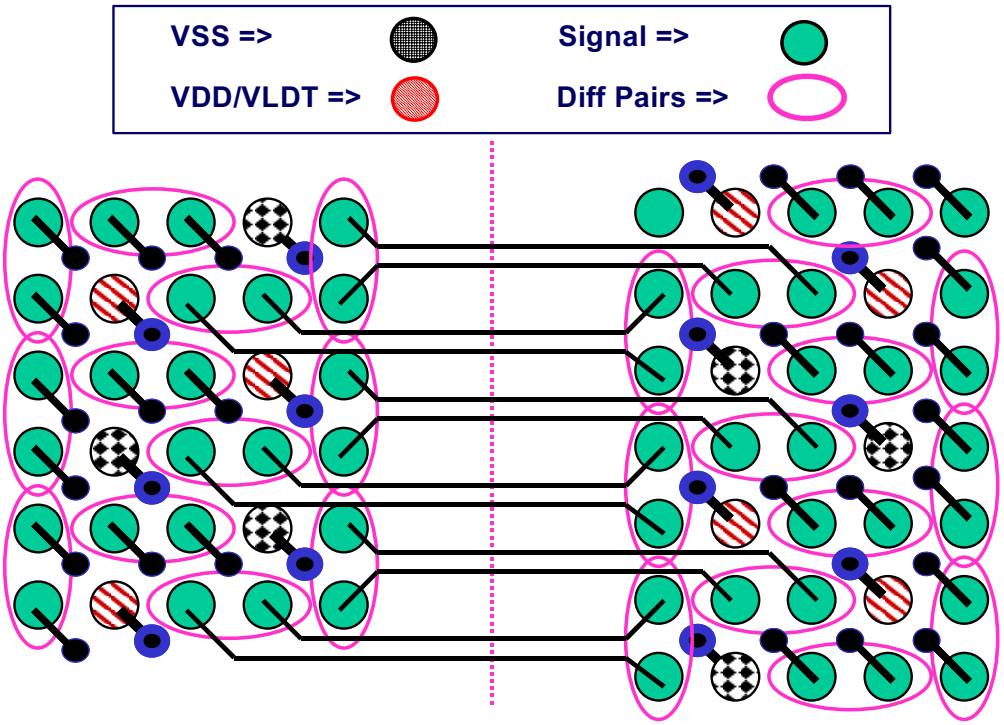


Figure 32. Two-Signal-Layer Routing Example—Top Layer

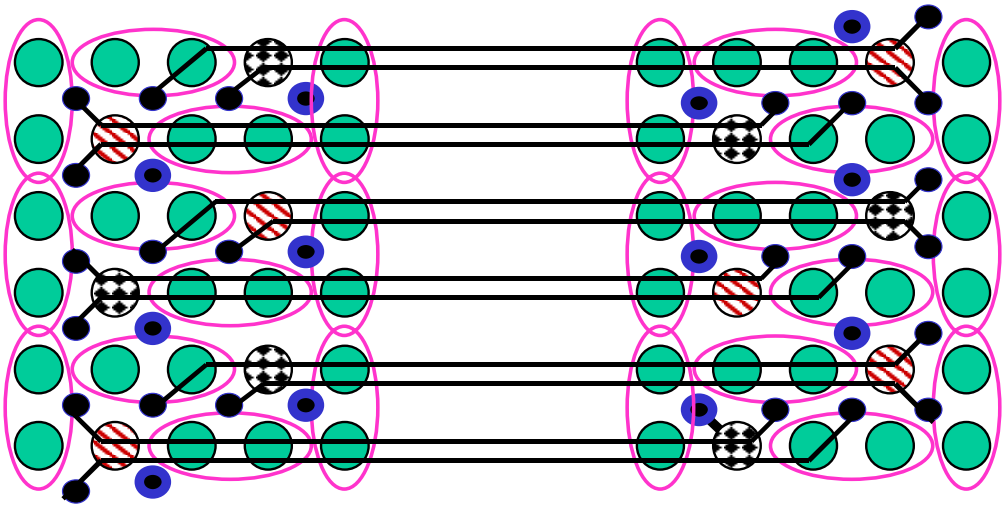


Figure 33. Two-Signal-Layer Routing Example—Bottom Layer

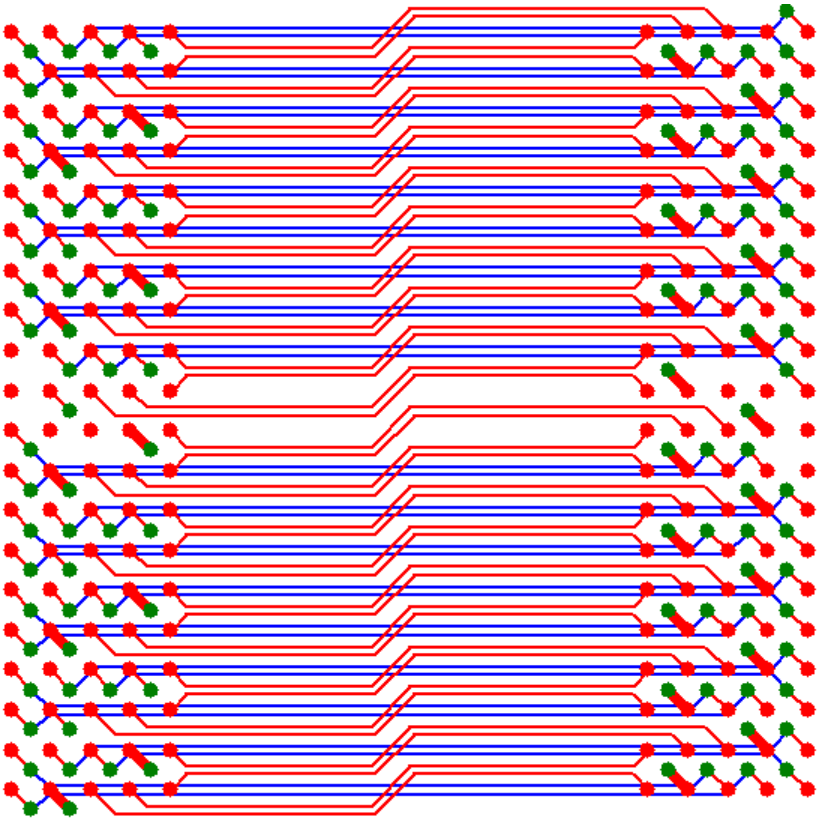


Figure 34. 16x16-Bit Route Example

3 Power Distribution Design Guide

3.1 HyperTransport Power Delivery System

A practical HyperTransport power distribution network will include the on-die decoupling capacitance, package and motherboard interconnects, optional on-package and on-motherboard discrete decoupling capacitors, as well as the voltage regulator with the associated bulk decoupling capacitors. Because the HyperTransport power supply is not as demanding as the core supply or the supplies for other I/O interfaces, several layout alternatives may be used in the design. However, since HyperTransport is a very high data-rate I/O interface, careful design practices must be exercised to ensure a low DC and AC impedance path from the regulator to the die.

Unlike other I/O interfaces, the HyperTransport interface may consist of several independent HyperTransport links on a single die. The power to each link on the die must be delivered through the package by an independent interconnect in order to provide maximum isolation between the individual links. This will minimize the high frequency noise on the individual HyperTransport supply due to the switching of high data-rate signals on other HyperTransport links.

3.2 Power Supply Impedance Basics

A typical equivalent circuit for the HyperTransport power interconnect that can be used to estimate the impedance at the die is shown in Figure 35. It consists of an on-die capacitance, wirebonds/flip-chip bumps and vias/balls/pins through the package, planes in the package, on-board decoupling capacitors, and the motherboard. The values of the equivalent lumped elements in the circuit are normally extracted with the help of applicable analytical formulas or 3-D field solvers.

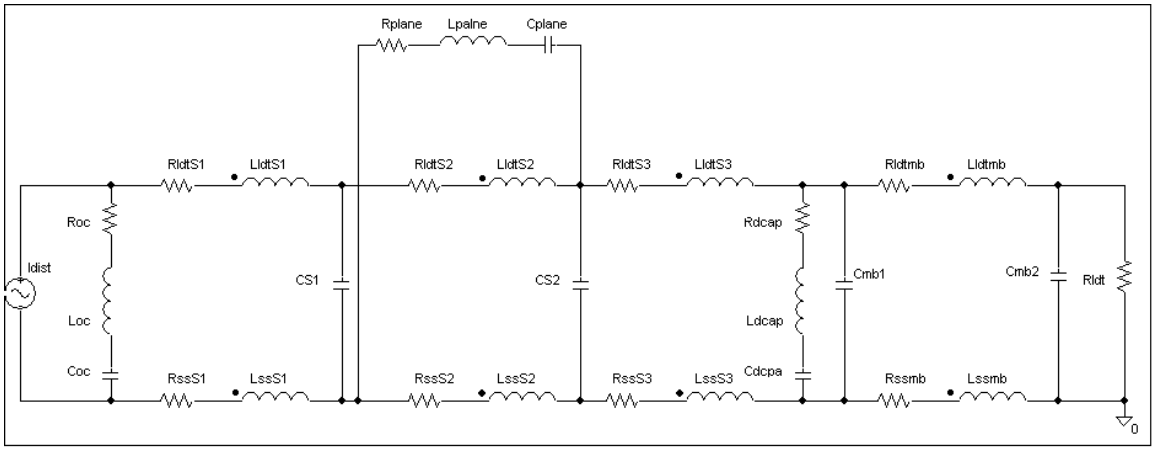
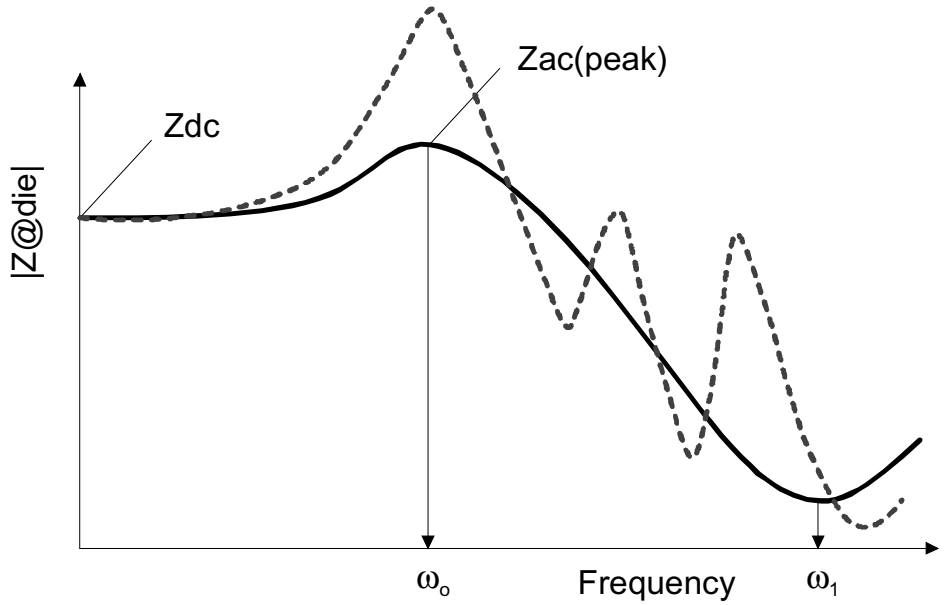


Figure 35. Equivalent Circuit of Power Interconnect from Regulator to Die

The equivalent circuit model of the HyperTransport power interconnect, produces an impedance profile shown in Figure 36. Notable characteristics relevant to the design are the DC impedance, mid-frequency

peak (at ω_o), and the high frequency point (ω_1) after which the impedance starts increasing. The DC and low frequency impedance are dominated by the resistance of the HyperTransport interconnect and can be estimated from the conductivity and the geometry of the metallization. The mid-frequency peak at ω_o is determined by the overall loop inductance of the interconnect (all Ls in circuit of Figure 35) and the on-die capacitance. Finally, the location of the high frequency null at ω_1 is driven by the on-die capacitance (C_{OC}) and the parasitic inductance (L_{OC}) associated with it.



Notes: Solid line = Desirable. Dashed line = Undesirable

Figure 36. Impedance of Power Interconnect at the Die

It is important to point out that the HyperTransport impedance profile shown in Figure 36 (solid line) is typical of a well-designed delivery system. The peak AC impedance is meeting the performance targets and is not much higher than the DC impedance which implies that the supply has a low Q. Moreover, at high frequencies (beyond ω_o) the impedance remains much lower than its DC value. A poorly designed power delivery network will exhibit an impedance profile (dashed line) with a high-Q and a resonant response (consisting of multiple peaks) at high frequencies. This implies that the power supply impedance seen at the die will result in unacceptably high voltage drop across it and will amplify high frequency noise generated by the switching HyperTransport driver and/or receiver circuits.

3.3 Selection of Performance Target

The power supply impedance can be used as a metric for assessing if a specific design meets the performance targets. This is done by defining the maximum impedance that the power delivery system can have, given the maximum supply voltage variation at the die and the maximum (DC + AC) current drawn by the die. For example, if 10% variation from the nominal voltage is acceptable and the maximum expected current draw is I_{MAX}, then:

$Z_{MAX} = 0.1 * V_{NOMINAL}/I_{MAX}$

Once Z_{MAX} is estimated, the impedance profile at the die of the power delivery system cannot exceed this value over the entire frequency range of operation. This frequency range is determined by the highest frequency components of the HyperTransport signals to which the power supply will be exposed during operation.

3.4 Device Design Guidelines

3.4.1 On-Die Decoupling Recommendations

As stated previously, the on-die decoupling capacitance plays an important role in controlling the performance of the power delivery network at high frequencies. Higher values help achieve lower HyperTransport power supply impedance, by shifting the entire response towards DC and reducing the peak. Figure 37 illustrates the general properties of this effect.

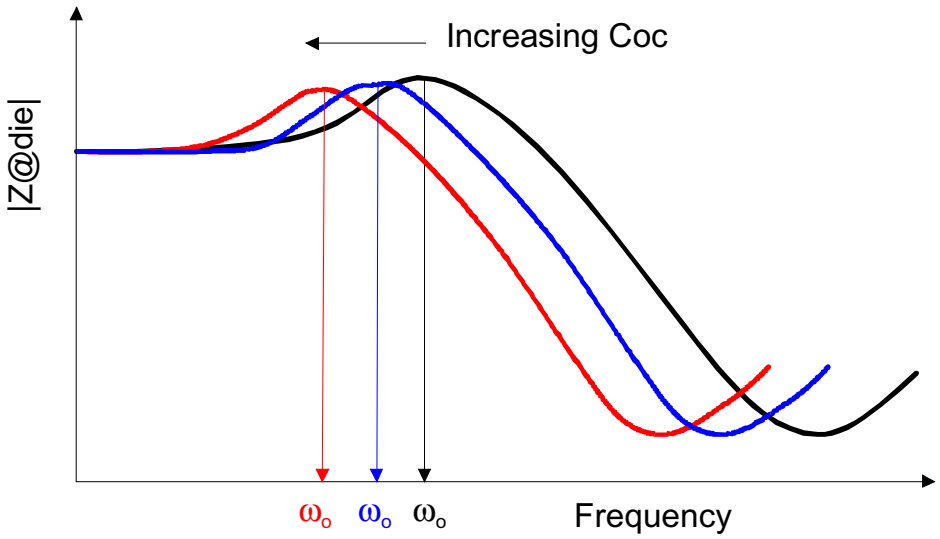


Figure 37. On-Die Capacitance Effect on Power Interconnect Impedance at the Die

For data rates below 800 MT/s, it is recommended that at least 200 pF of on-die decoupling capacitance be used per HyperTransport signal pair. This implies that for an 8-bit HyperTransport link, including the clocks and control signals, the on-die decoupling capacitance should be at least 2.4 nF. These values should be doubled for HyperTransport links operating at data rates of 800 MT/s and above.

3.5 Device Package Design Guidelines

The following discussion will focus on chipset packages that are intended for use in platforms with minimum motherboard resources (such as four metal layers and no backside components), because they represent the greatest design challenge. Moreover, the HyperTransport signal routing standards do not allow the VLDT power connections to be interspersed in the HyperTransport signal field of the package footprint. As a result, the VLDT power balls can only be located outside the HyperTransport signal block as shown in Figure 38, thereby posing additional constrains on package design.

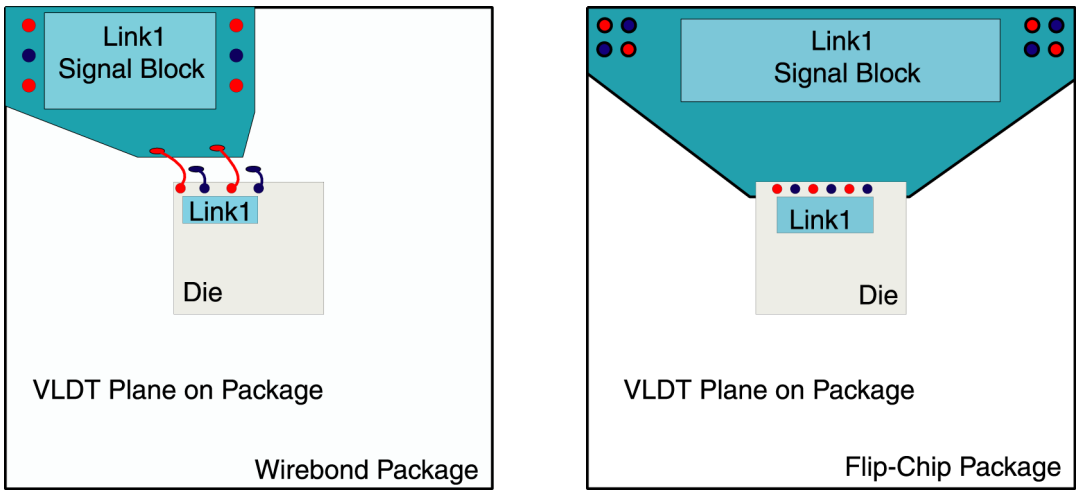


Figure 38. Typical Locations of VLDT Power Connections outside the Signal Block

3.5.1 Wirebond versus Flip-Chip Packages

HyperTransport technology can be packaged in either ceramic or organic substrates. Typically, chipset packages are plastic BGAs with the die wirebonded to them. Depending on the body size, some packages will also have a partially depopulated footprint. All these factors tend to limit the performance of the package (and the power delivery system), especially for high data-rate I/O interfaces, unless a large number of package resources (planes, vias, balls, and wirebonds) are devoted to them. This makes designing a reliable power supply interconnect on the package difficult.

One way to improve the performance is to use flip-chip packages and fully populate the footprint. This will automatically reduce the power delivery system impedance due to the increased number of package resources and elimination of wirebonds. Another benefit of flip-chip technology is it allows the HyperTransport power connections to be made directly under the die. To achieve higher performance power delivery solutions, especially for chipsets with very fast HyperTransport interfaces (i.e., 800 MT/s and above), preference should be given to using flip-chip technology in favor of wirebond technology.

3.5.2 Package Resource Allocation

The layout of the HyperTransport power supply interconnect on the package should have sufficient resources to ensure low DC and AC impedance. To help accomplish this, the following sections offer recommended package resource allocations.

3.5.2.1 Balls and Internal Vias

If the chipsets are being designed to support HyperTransport interfaces for data transfers below 800 Mbits/s, then wirebond technology can provide a practical packaging solution. For data transfer rates of 400 Mbits/s at least four balls should be dedicated to a single HyperTransport link to connect the VLDT power supply between the package and the motherboard. For all chipsets intended for operation at 600 Mbits/s, this number should be increased to eight. All VLDT balls should be located near the ground balls to provide a nearby current return path and to keep the loop inductance low (see Figure 39). A low

impedance return path is even more critical in high-performance applications and may require more than a single ground ball per VLDT ball.

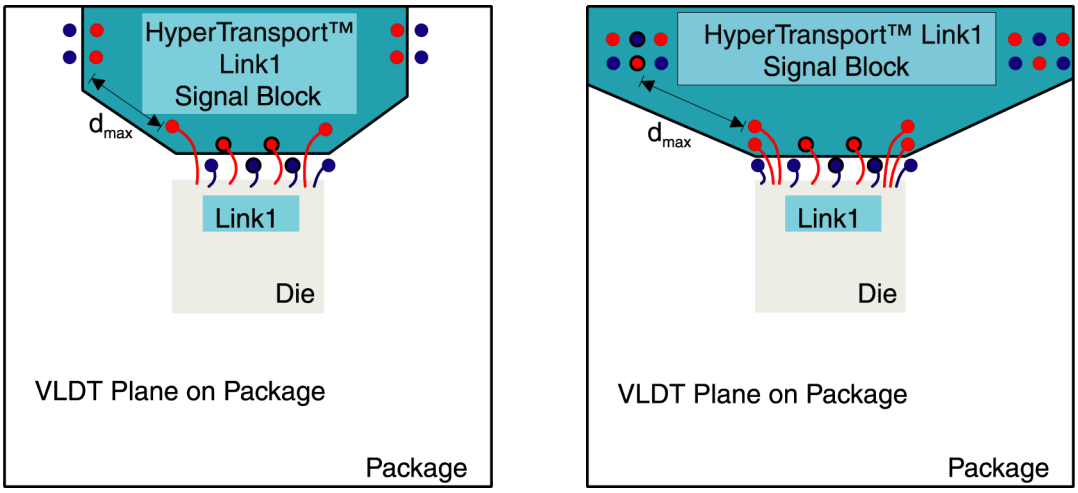


Figure 39. VLDT Interconnects for Wirebond Packages

The spacing between the VLDT balls and the wirebond connections to the plane should be relatively small (no more than three ball-pitches wide) to keep the inductance low. It is assumed that the VLDT connections to the motherboard are the perimeter of the package. However, depending on the size of the VLDT plane, the spacing d_{max} may need to be increased. The effects of larger d_{max} should be compensated by increasing the number of VDLT balls and wirebond connections to the die (left-side graphic in Figure 39).

Unlike the balls, internal via resources are more readily available. Consequently, the number of VLDT vias internal to the package substrate should be as large as possible. For organic substrates with wirebond die-attach, the minimum number of plated through holes (PTHs) should be dictated by the number of wirebonds. Specifically, it is recommended there be at least one PTH for every VLDT wirebond (see subsequent sections for wirebond recommendations). In the ceramic substrates this ratio should be increased to 3:1 since the impedance of the internal tungsten vias is considerably higher than the impedance of the copper PTHs.

Package design involving flip-chip technology should follow the same guidelines for the minimum numbers of internal vias as previously suggested. However, whenever possible, the number of internal vias should be increased within the practical limitations of available package resources, especially for faster and wider (16-bit) HyperTransport interfaces.

3.5.2.2 Planes

In wirebond packages, large sections of a plane should be used to distribute the VLDT inside the package, as is depicted in Figure 39. The use of straps (narrow metal stripes) to make connections between the balls and vias inside the wirebond package should be avoided, because this will lead to unacceptably high DC resistance as well as high inductance of the power supply interconnect. If the package contains multiple power planes, then a section for VLDT should be dedicated on each power plane, especially for packages supporting faster HyperTransport interfaces.

The guideline for selecting the minimum size of the plane for VLDT is based on two factors:

- The physical layout of the HyperTransport signal block on the package, which is determined by the speed and the size (8 versus 16 bits) of the HyperTransport link.
- The number of VLDT and associated ground balls required for a low-impedance connection to the motherboard.

Unlike wirebond packages, VLDT interconnects in flip-chip packages may be in the form of a plane or strap, as illustrated in Figure 40. The increased impedance of the strap interconnect is partially compensated by the direct and low impedance connections from the die to the VLDT metallization in the package, making the strap a sub-optimal but viable alternative to a large section of a plane.

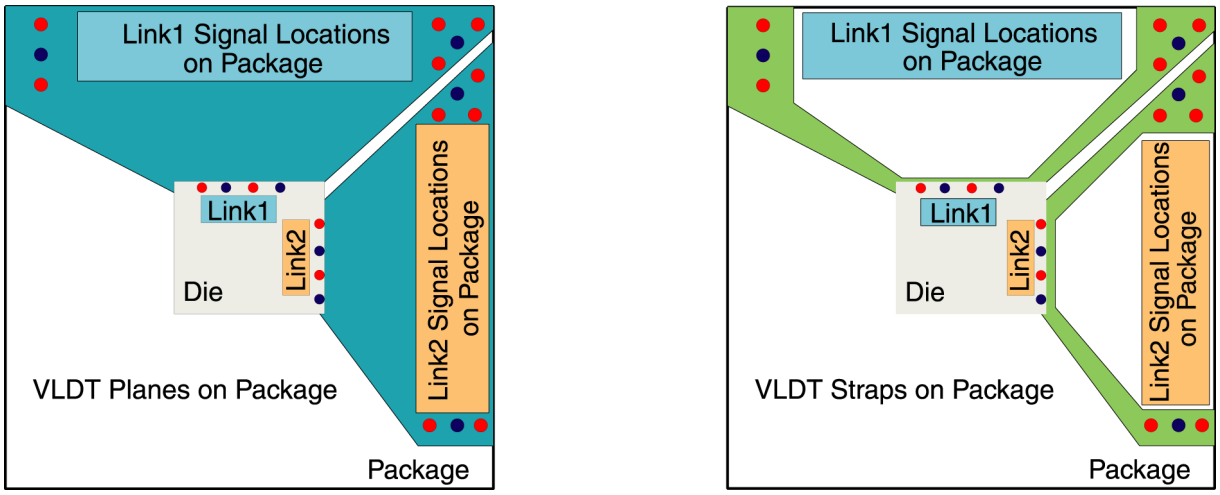


Figure 40. VLDT Interconnects for Flip-Chip Packages

If decoupling capacitors for VLDT will be used on the package, then the VLDT plane in the stack-up should be as close to the top surface on the package as possible (to make short via connections from the capacitors to the plane). In addition, the area of the plane between the die and the capacitor connections to the VLDT plane should include minimal perforation.

3.5.2.3 Connections to the Die

If wirebonds are used to deliver VLDT to the die, then a minimum of six wirebonds should be allocated per 8x8-bit 400 MT/s HyperTransport link. Each VLDT wirebond should be as short as possible and have a nearby VSS wirebond that functions to keep the VLDT-ground wirebond loop inductance to a minimum. This is very important for wirebond packages because the wirebond parasitic resistance and inductance are the largest contributing factors to the power interconnect impedance.

The use of flip-chip technology inherently eliminates large parasitic impedances of the wirebonds. Moreover, it allows making VLDT connections directly under the die rather than around its perimeter, as the comparison in Figure 41 illustrates.

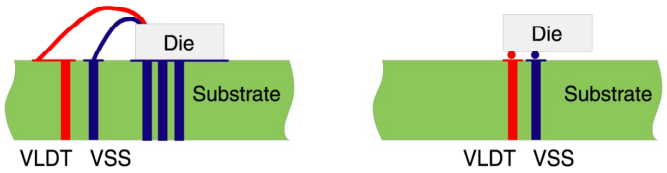


Figure 41. Differences in VLDT Interconnect for Wirebond and Flip-Chip Technologies

The flip-chip die attachment yields considerably lower impedance for the HyperTransport supply current and makes it more immune to the noise generated by the switching of high data-rate circuits. Consequently, flip-chip packaging is the recommended choice for all chipsets supporting data rates of 800 Mbits/s and above.

3.5.3 On-Package Decoupling Capacitors

The use of discrete chip capacitors on the package should be considered for high-performance applications. These applications may include chipsets supporting very fast HyperTransport interfaces of 1.2 Gbits/s and above, with multiple HyperTransport links, some being 16-bit wide.

If the capacitors are required, their quantity and values should be selected based on having a circuit model for the entire power delivery system. However, if the model is not available, then the following options should be considered:

- One 100–220 nF capacitor and one 10–22 nF capacitor.
- Capacitors should be of X7R variety, and their size should be driven by the signal routing on the package (0603 or 0508 will work best).
- Capacitors should be as close to the VLDT-side of the die as possible and be connected to a section of the VLDT plane with fewest perforations between the capacitor connections and the die.
- There should be as many vias as possible from the capacitor pads to the VLDT plane.

Note that the recommended discrete capacitors are effective at frequencies between 10 and 100 MHz. Their functionality is to reduce the mid-frequency peak of the interconnect impedance at the die (ω_o in Figure 36). They are ineffective at higher frequencies (even the 39 pF capacitors), because the parasitic inductance associated with the vias connected them to the VLDT plane and the path from the vias (on the plane) to the die is too high. Finally, the use of higher valued capacitors than those recommended in this section is not advised, because this is not likely to yield improved performance.

3.6 Motherboard Design Guidelines

Many motherboards on which the chipsets supporting HyperTransport will be used are expected to have four layers. However, in other platforms, the motherboards may be six to eight layers thick. The motherboard resources will affect the chipset package design. For example, the number of layers in the motherboard will dictate if VLDT is routed on the board as a trace or will be a large section of a plane. Larger number of layers will also alleviate some of the signal routing constraints, allowing for placing a greater number of discrete decoupling capacitors closer to the chipset packages or even on the back of the board.

Clearly, the added motherboard resources will improve the performance of the overall VLDT power delivery system. However, if the chipsets are used on the standard four-layer boards, resources for VLDT are far more limited and must be used optimally.

3.6.1 VLDT Layout

Irrespective of the number of layers in the motherboard, the HyperTransport voltage regulator should be as close to the chipset package as possible. The maximum recommended distance is 1.5–2.0 inches. If possible, such as in six- or eight-layer motherboards, a section of a plane on one of the inner signal layers should be used to deliver VLDT to the package. This plane should be large enough to accommodate the placement of all VLDT regulator components and to make connections to every VLDT ball on the chipset package, as shown on the left side of Figure 42.

In four-layer motherboards, due to signal routing constrains, VLDT is likely to be routed to the package on the signal layer as a trace (see Figure 42). As such, the VLDT trace can only be connected to a subset of VLDT balls on the package, which are on either side of the HyperTransport signal block. The intent of such an interconnect scheme is to provide maximum flexibility for component placement and signal routing on the motherboard. For clarity, in the remainder of this document, the side of the HyperTransport signal block to which the trace from the regulator is attached directly to the VLDT balls is referred to as connected. In such cases, the other side of the block is referred to as unconnected. For details, see the graphic on the right side of Figure 42.

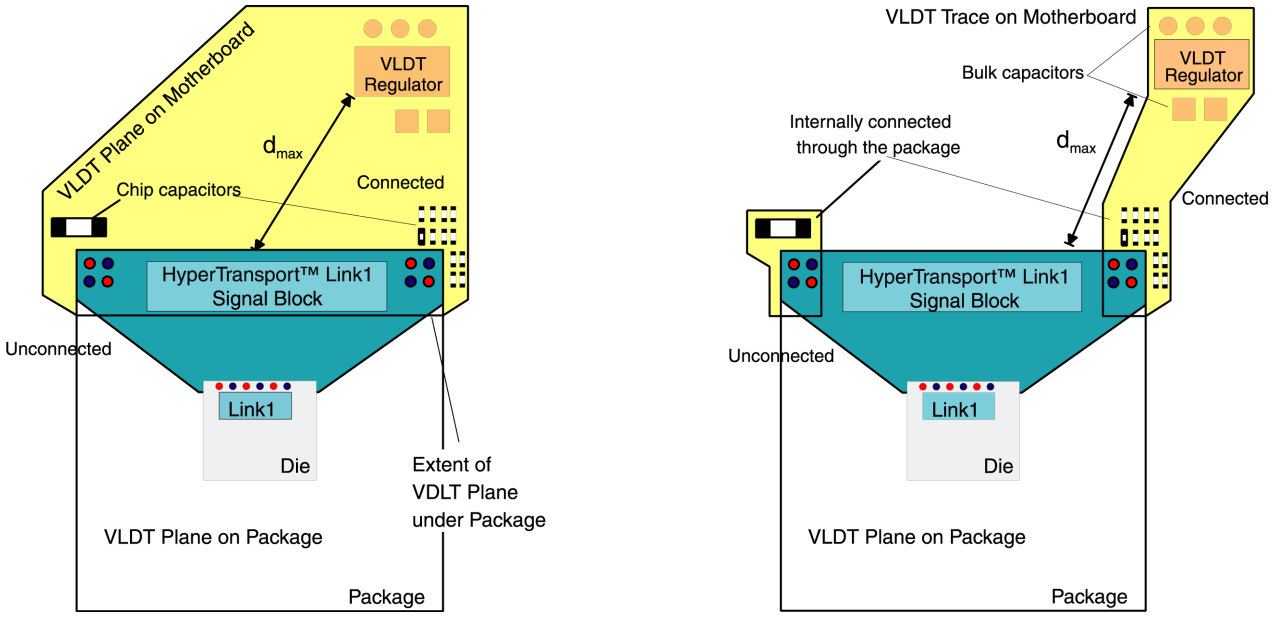


Figure 42. Recommended Motherboard Layout Options for VLDT

It is important to stress that although the VLDT connection from the motherboard is only made on a single side of the signal block, all of the VLDT balls on both sides of the HyperTransport block are connected within the package. The VLDT balls that are not connected directly to the regulator by the trace on the motherboard should not be left unterminated. A decoupling capacitor must be placed on the motherboard at the unconnected side of the HyperTransport signal block as close to the package as possible. The specific recommendations for the capacitor values will be given in Section 3.6.2.

The minimum width of the trace should be 0.2 inches or greater whenever possible. However, irrespective of the width of the trace, this motherboard interconnect design solution should be properly decoupled on the motherboard, especially for any HyperTransport interface of 800 Mbits/s and above.

In general, the use of the plane section for VLDT leads to considerably lower impedance of the VLDT and VSS (ground) plane pair, compared to the impedance of the trace (VLDT) and plane (VSS) combination. In addition, the availability of greater VLDT metallization area also allows for placing a greater number of capacitors near the package.

3.6.2 Decoupling Capacitors

The use of the decoupling capacitors on the motherboard is strongly recommended. For optimal VLDT performance, several discrete components are required. They should be placed as close as possible to the package, without interfering with the signal routing. This can be implemented with an array of 0603-size capacitors, as shown in Figure 43(L). If the application permits, the capacitors should be mounted on the back of the motherboard, directly under the section of the die containing the HyperTransport link.

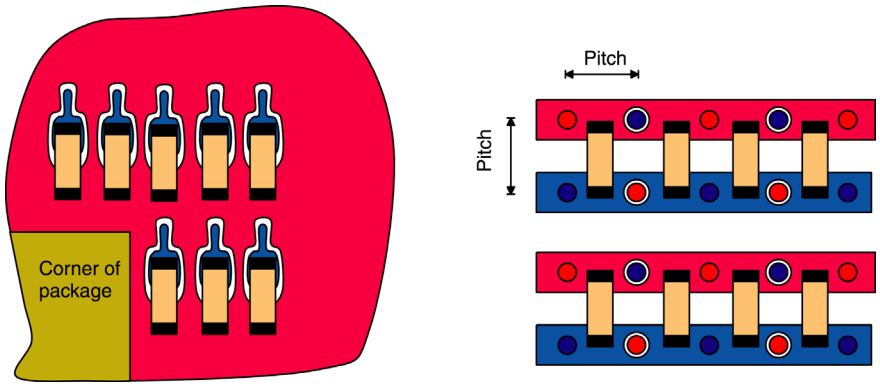


Figure 43. Decoupling Capacitor Array: Motherboard Topside(L) and Backside(R)

The pitch of the backside capacitor array shown in Figure 43(R) should be determined by the motherboard PTH, board component assembly, and soldering design rules.

The best way to select the number of capacitors and their values is through SPICE simulations, if the circuit model for the power delivery system is available. However, if the circuit model is unavailable, then the following guidelines should be used for component selection:

Option 1: Without On-Package Capacitors

The total number of capacitors on (or near) the trace should be at least nine:

- Two capacitors should be 220–330 nF.
- Four capacitors should be 20–33 nF.
- Three capacitors should be 5–10 nF.

- All capacitors should be of X7R variety.
- A single 4.7 µF 1206 X7R capacitor should be used to terminate the unconnected side of the HyperTransport link.

Option 2: With On-Package Capacitors

If the package includes capacitors recommended in Section 3.5.3, then a minimum of four capacitors should be sufficient to ensure adequate decoupling of the connected side of the link at mid frequencies. The board-level component values should be selected from the list of Option 1, not repeating the same capacitor values as those already mounted on the package.

For example, if the on package capacitors are 220–330 nF (typically high-valued capacitors would be placed on the package), motherboard decoupling would consist of two 5–10 nF capacitors and two 20–33 nF capacitors.

The unconnected side of the link must still be terminated with a 4.7 µF 1206 X7R capacitor.

3.6.3 Bulk Decoupling

It is important to add that proper bulk decoupling is required for stable operation of the regulator and to ensure low-power delivery system impedance at low frequencies. Typically, approximately 1500 µF is required to achieve such targets. It is recommended that low ESR OsCon, Aluminum Polymer, or equivalent type capacitors be used for bulk decoupling.

3.6.4 Single HyperTransport Link versus Multiple HyperTransport Links

The previous discussion dealt primarily with design aspects of the power delivery system for chipsets that support a single HyperTransport link. Many of the topics covered also apply to chipsets supporting multiple HyperTransport interfaces. However, whenever the application calls for multiple HyperTransport links, a different approach of laying out the HyperTransport power interconnects on the package and motherboard must be followed.

Specifically, if the chipset supports only a single HyperTransport I/O interface (single link), it is sufficient to have a single electrical path to bring the power to the die, as shown in Figure 44. It is recommended that large sections of the plane be used to make the connections to the package whenever possible.

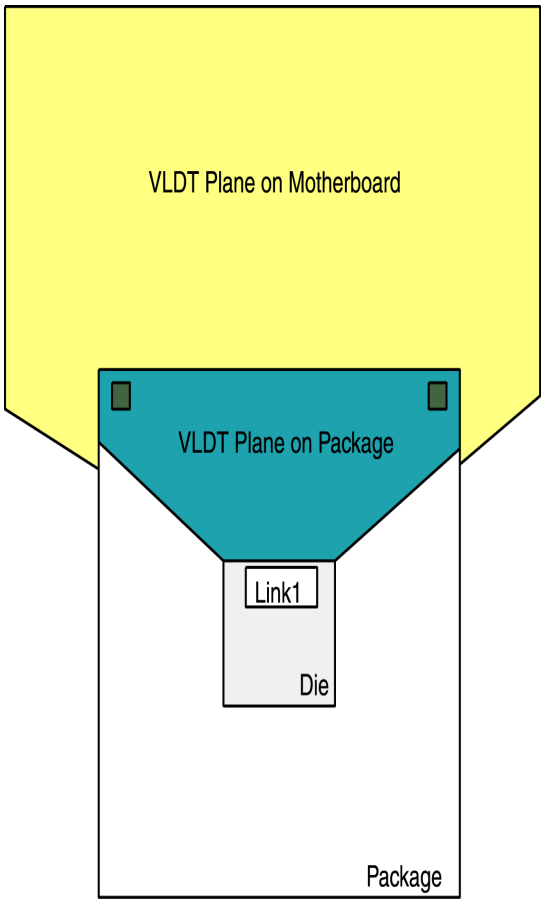


Figure 44. Power Supply Interconnect for a Single HyperTransport Link

However, if the chipset has to support multiple HyperTransport links, then a separate power supply interconnect for each link must be provided on the package, as illustrated in Figure 45. In cases where this supply layout on the motherboard may not be possible, a single VLDT regulator may be used to supply the power to multiple HyperTransport links on the die, as shown on the right in Figure 45. The distance from the regulator to the chipset package (d_{max}) should not exceed 1.5–2.0 inches.

Note that although a single voltage regulator can be used to feed two independent HyperTransport links, the motherboard routing must consist of two separate traces leading from the regulator to the package as shown in Figure 45. The traces should be 0.2 inches wide and run separately for a minimum length (l_{max}) of at least 1.0 inch. The minimum spacing between them should not be less than 0.1 inch. If these layout recommendations are not followed, significant coupling can be expected between the VLDT links if they are connected to the same regulator.

It is not recommended that a single voltage regulator be used to feed more than two HyperTransport links in any application.

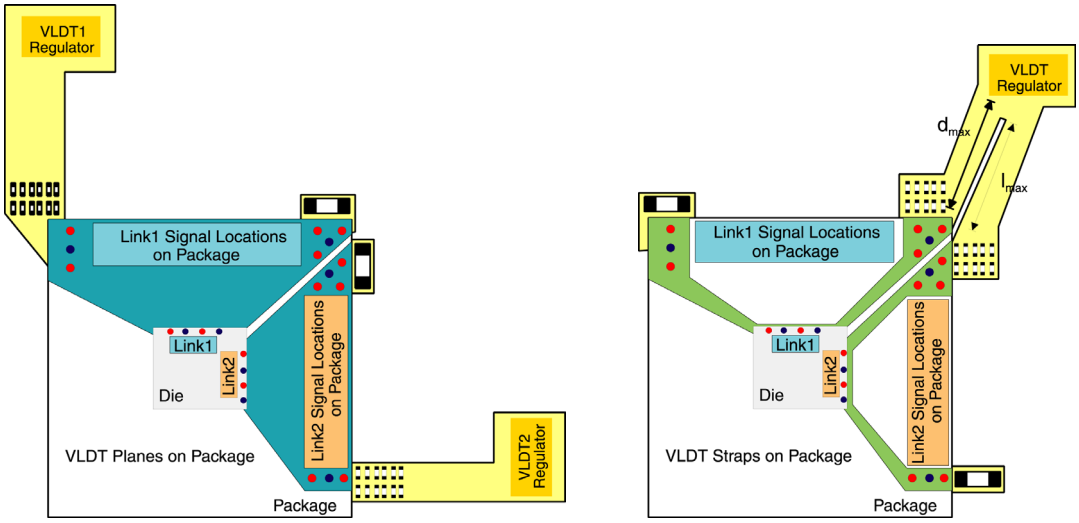


Figure 45. Connecting Power Supplies to Packages with Multiple Links

Regardless of which connection scheme is used to deliver power to HyperTransport interfaces on the package, it is recommended that decoupling capacitors be placed at the point where the traces connect to the package as well as at the unconnected side of the corresponding section of the VLDT plane or strap. For optimum utilization of the capacitors, it is recommended that the lower-valued capacitors be placed near the trace, while the higher-valued capacitors be placed at the other side of the plane (or the unconnected corner of the package).

The number of the discrete components and their capacitance values should be selected based on performing simulations using an equivalent circuit model for the specific HyperTransport power supply interconnect (package technology (organic or ceramic) and construction (number of layers, via, ball, and flip-chip bump resources), motherboard, etc.). If the model is unavailable, then it becomes very difficult to provide such information. However, as a general rule the following guideline may be followed to obtain reasonable performance.

Near the trace from the regulator location, use at least four capacitors:

- Select the low-valued capacitors such that they have an ESR value of approximately 1.0 Ω.
- Two 10–22 nF capacitors.
- Two 1–5 nF capacitors.
- All capacitors should be of 0603 X7R variety and mounted as close as possible to the package.
- A single 4.7 µF 1206 X7R capacitor must be placed at the unconnected side of the VLDT plane/strap interconnect in the package.